Input Current Balancing Control Method under Imbalanced Load for Three-phase Multi-port Converter based on Modular Multilevel Converter

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***Abstract*— This paper proposes a balancing control method for imbalanced load in multi-port converter based on a modular multilevel converter (MMC) topology. In the multi-port converter with imbalanced loads, the three-phase current is balanced by dividing voltage among the cells. However, the multi-port converter has a limitation of the compensation capability for the imbalanced load. This paper clarifies the theoretical limitation with the proposed divided voltage method of the compensation capability of the imbalanced load. The proposed method is demonstrated by a 200-V, 17-kW laboratory system in order to show the validity of the proposed method. In spite of the load imbalance, balanced three-phase input current is achieved and DC link voltage error becomes 0.11%.**

Keywords*— *modular multilevel converter, multi-port converter, power distribution, balancing control

I. Introduction

In recent years, the energy storage with large-capacity and small-volume such as lithium-ion cells and supercapacitors have been developed due to an increasing demand of electric vehicle [1]-[2]. These large batteries are built using many modules that, although nominally identical, need to be controlled independently according to their individual condition. Accordingly, multi-input and multi-output converters for the batteries control each source and load independently [3]-[4]. Since the output voltage of the batteries is relatively small, the step-up transformer is required for these multi-port converter in order to interconnect the medium voltage grid. However, the step-up transformer increases the total volume of the system. In addition, the capacity of the system is limited by the capacity of the step-up transformer. Hence, these multi-port converters are not suitable for the large-scale battery chargers. In order to overcome the above problems, the multi-port converter using a modular multilevel converter (MMC) topology has been proposed for large-capacity multi-port battery charger [5]-[6], battery energy storage system (BESS) [7]-[8], and so on [9].

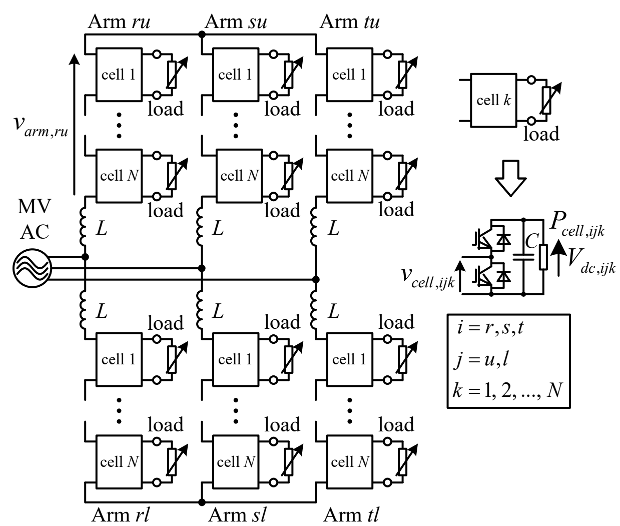


Fig. 1. Concept of multi-port converter based on MMC.

Fig. 1 shows a concept of a multi-port converter based on MMC with double-star chopper-cells [10]. The cells of MMC are utilized as input and output ports. Each cell is connected to the load as shown in Fig. 1 because this paper considers only charging operation of the multi-port converter. Since the multi-port converter based on MMC is directly connected to the medium voltage grid without the line frequency transformer, it reduces both the system volume and the system weight compared with those of the conventional system with the transformer [11]-[13]. The multi-port converter is required to interchange the power between the cells in order to obtain balanced three-phase current, because the batteries connected to the cells have different charging requirements [5]-[9]. The multi-port converter based on MMC has a limitation of the compensation capability for the load imbalance in one arm [5]. In Ref. [5]-[6], the compensation for the imbalanced load in one arm is achieved. However, in these papers, the compensation capability for the load imbalance has not been revealed theoretically. Although an additional circulating current extends the operation range of compensation for imbalanced load in one arm, the load conditions to need the additional circulating current is not described in Ref. [5]. Therefore, even in the condition that an additional circulating current is not necessary, the additional circulating current will flow, which results in increases of switching loss and conduction loss.

This paper proposes the input current balancing method without any additional circulating current in the three-phase MMC in spite of the imbalanced load condition in one arm. Therefore, the proposed method suppresses the current flowing the arm and reduces the switching and the conduction loss. In addition, this paper clarifies the limitation of the compensation capability of the load imbalance in one arm under no injection of the additional circulating current. This paper is organized as follows; first in section II, the control method is introduced, and the limitation of the compensation capability for the load imbalance in one arm is clarified theoretically. Next, in section III, the validity of the proposed control is confirmed by the simulation. Finally, in section IV, the proposed control is confirmed by the experiment with 17-kW prototype.

II. Control Strategy for Multi-port Converter

A. Definition of variables

The sum of output power of all cells in the arm-*ij* is defined as $P_{arm,ij}$. In addition, the average DC link voltage of cells in one arm $V_{dc,arm,ij}$, the averaged DC link voltage of all cells in the multi-port converter $V_{dc,tot}$, and the averaged DC link voltage of cells in *i*-phase $V_{dc,ph,i}$ are defined as,

$$V_{dc,arm,ij} = \frac{1}{N}\sum_{k=1}^{N} V_{dc,ijk}, \quad (i=r,s,t,\ j=u,l) \tag{1}$$

$$V_{dc,tot} = \frac{1}{6}\sum_{\substack{i=r,s,t\\ j=u,l}} V_{dc,arm,ij} = \frac{1}{6}\sum_{\substack{i=r,s,t\\ j=u,l}}\left(\frac{1}{N}\sum_{k=1}^{N} V_{dc,ijk}\right) \tag{2}$$

$$V_{dc,ph,i} = \frac{1}{2}\sum_{j=u,l} V_{dc,arm,ij} = \frac{1}{2}\sum_{j=u,l}\left(\frac{1}{N}\sum_{k=1}^{N} V_{dc,ijk}\right), \quad (i=r,s,t) \tag{3}$$

In the multi-port converter, the grid phase voltage is applied into each arm for the AC-DC converter operation with the balanced input current. In addition, the arm voltage command v_{arm}^{*} includes a DC voltage because of the chopper-cell of the multi-port converter [12]-[13]. Therefore, the command of the arm voltage $v_{arm,iu}^{*}$ for upper arm in *i*-phase is assumed to consist of the DC component and the grid frequency component as in (4),

$$v_{arm,iu}(t) = \frac{NV_{dc}}{2} - \sqrt{2}V_g\cos\left(2\pi f_g t\right) \tag{4}$$

where V_{dc} is a DC link voltage of the cell, V_g is an RMS value of the grid phase voltage, and ω_g is an angular frequency of the grid. The phase of the grid frequency component of the arm voltage $v_{arm,il}^{*}$ for lower arm in *i*-phase is reversed from that of the upper arm. In addition, the arm voltage is always positive because the chopper-cells cannot output negative voltage.

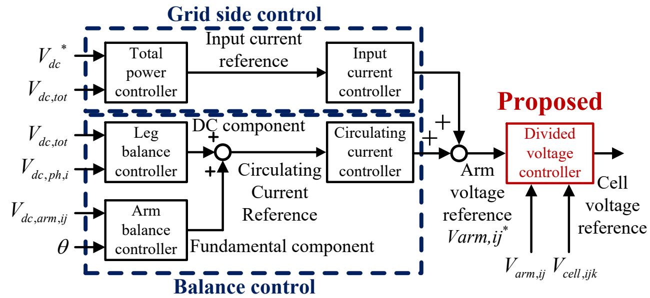


Fig. 2. Outline of control strategy for multi-port converter.

The voltage redundancy ρ is defined for the theoretical analysis in this paper. The voltage redundancy ρ is expressed as the sum of the DC link voltage of cells in one arm divided by the peak-to-peak value of the arm voltage v_{arm} as in (5),

$$\rho = \frac{NV_{dc}}{2\sqrt{2}V_g}. \tag{5}$$

When any zero-phase voltage injection is not utilized and the arm voltage is expressed in (6), the voltage redundancy ρ must be larger than 1 [13]. On the other hand, when some zero-phase voltage for the arm voltage $v_{arm,ij}$ is utilized, the voltage redundancy ρ can be smaller than 1, which is the case for the multi-port converter.

B. Control method for power distribution between cells

Fig. 2 shows an outline of the control block diagram for the multi-port converter. The grid side control part and the balance control part are a control method adopted in the conventional MMC [5], [14]. In this paper, the divided voltage controller is proposed. All controllers shown in Fig. 2 adopts PI controller.

Fig. 3 depicts the detailed control block diagrams for the multi-port converter. The grid side control part as shown in Fig. 3 (a) is implemented for the balanced three-phase input current. The output of the total power controller is a command of the active part of the input current and proportional to the total output power of the multi-port converter. The output of the total power controller is input to the input current controller.

Fig. 3 (b) depicts the balance control part of the control. The balance control part controls the circulating current to compensate the load imbalance between the phases and the upper and lower arms. In this paper, the DC component and the grid frequency component are utilized as the circulating current for the compensation of the load imbalance between the arms, whereas higher harmonic current than them is not utilized to compensate the load imbalance in one arm. The leg balance controller regulates the average value of the DC link voltages of the cells in one phase by interchanging the power between phases. The outputs of the leg balance controllers are three commands of DC circulating current, which are for *r*-, *s*-, and *t*-phase, respectively. An active power is generated by the DC component of the circulating current $I_{dc,i}$ and the DC component of the arm voltage v_{arm} in (4).

The arm balance controller in Fig. 3 (b) regulates the averaged DC link voltages of the cells in the arms by interchanging the power between the upper and lower arms. The output of the arm balance controller is the grid frequency component of the circulating current $i_{\omega,i}$. The arm balance controller in Fig. 2 (c) utilizes three components; the active part of the positive sequence Re[$I_{+\omega}$], active part of the negative sequence Re[$I_{-\omega}$], and the reactive part of the negative sequence Im[$I_{-\omega}$] of the grid frequency component of the circulating current [5], [14]. The control loop of the arm balance controller is implemented by adopting one *rst-αβ0* transformation and two *dq-rst* transformation as shown in Fig. 2 (c) [5].

A sum of the output of the leg balance controller $I_{dc,i}^*$ and the output of the arm balance controller i_ω^* is input to the circulating current controller. The circulating current consists of the DC component and the fundamental component. In this paper, no additional circulating current for the compensation of the load imbalance in one arm is injected. Note that the zero sequence of the circulating current is zero because any zero sequence component cannot flow through the multi-port converter based on MMC due to the circuit configuration as shown in Fig. 1.

Finally, the sum of the outputs from the grid side control part and the balance control part is the command of the arm voltage v_{arm}^*, which is assumed as (4). The command of the arm voltage v_{arm}^* is input to the divided voltage controller to compensate the load imbalance in one arm and the command of the cell voltage $v_{cell,ijk}^*$ is obtained.

C. Proposed divided voltage controller

In this paper, the divided voltage controller is proposed in order to compensate the load imbalance between the cells in one arm. When the load connected to the cell is relatively large compared with the other cells in the same arm, the output voltage of the cell should be large in order to input a larger power to the cell. In contrast, the output voltage of the cell should be small when the load connected to the cell is relatively small. Thus, the command of the cell voltage is decided from the output powers of the cells in the converter. The output voltage of the cell $v_{cell,ijk}$ is written as,

$$v_{cell,ijk} = k_{ijk} v_{arm} = k_{ijk}\left(\frac{NV_{dc}}{2} - \sqrt{2}V_g \cos\omega_g t\right), \tag{6}$$

where k_{ijk} are coefficients, that are adjusted by the divided voltage controller in order to supply the desired power to each cell. The input power to the cell is expressed by the output voltage of the cell and the arm current i_{arm},

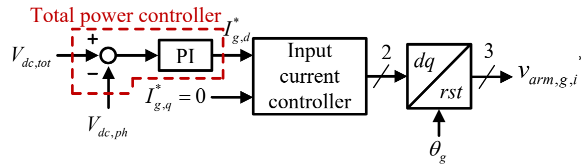
$$P_{cell,ijk} = \frac{1}{T_g}\int_0^{T_g} k_{ijk} v_{arm,ij} i_{arm,ij}\, dt = k_{ijk} P_{arm,ij}, \tag{7}$$

where T_g is the time period of grid voltage. The coefficient k_{ijk} is derived from (7) as,

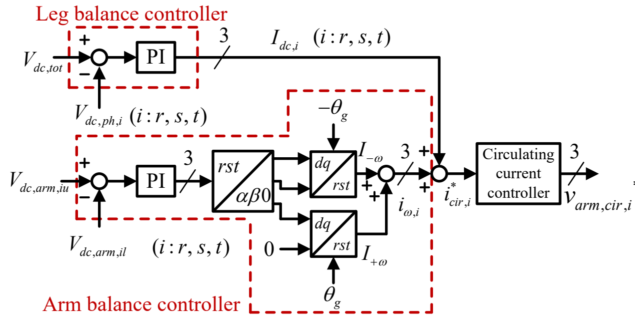
$$k_{ijk} = \frac{P_{cell,ijk}}{P_{arm,ij}} \tag{8}$$

The sum of the coefficient k_{ijk} in one arm is always 1. The coefficient k_{ijk} has a limitation in order to prevent the over-modulation of the cell voltage $v_{cell,ijk}$. As a result, the maximum input power to the cell is limited.

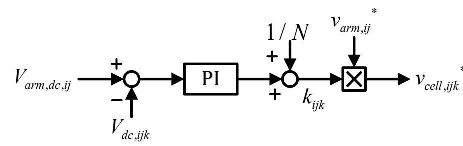
Fig. 3 (c) depicts a block diagram of the proposed divided voltage control. The divided voltage controller regulates the DC



(a) Grid side control part.



(b) Balance control part.



(c) Proposed divided voltage control.

Fig. 3. Detailed control block diagram for multi-port converter.

link voltage of each cell in one arm by using the PI controller. The command of the arm voltage is multiplied by the output of the PI controller. The output of the proposed divided voltage controller is the output voltage command of the cells. Phase-shifted PWM method is utilized in this paper. The phase-shifted PWM method has the merits of high equivalent switching frequency and more output voltage levels, which provide low total harmonic distortion (THD) compared with the other modulation methods. In addition, the semiconductor stress of each cell is evenly distributed [14].

Fig. 4 illustrates an example of the output voltage of cells with the proposed divided voltage method. As in Fig. 4, the third-order harmonic injection is used for the arm voltage v_{arm} in order to improve the voltage utilization factor in this paper. The proposed divided voltage method adjusts the command of the cell voltages in order to input the desired power to the cell as shown in Fig. 4. The sum of the cell voltages in one arm must be equal to the command of the arm voltage v_{arm}^*. As a result of the proposed method, the command of the cell voltage for the larger input power becomes large. On the other hand, the command of cell voltage for the smaller input power becomes small.

D. Limitation of compensation capability for load imbalance for divided voltage controller

This paper clarifies the limitation of the compensation capability of the proposed divided voltage controller for the load imbalance. The command of the cell voltage is decided by the output powers of the cells as shown in (6)-(8). In order to operate the converter without the over-modulation, there is a limitation of the compensation capability for the load imbalance in one arm. The minimum value of the output voltage of cells $v_{cell,ijk}$ has to be larger than zero as in (9). On the other hand, the maximum value of the output voltage of cells $v_{cell,ijk}$ has to be smaller than the DC link voltage of the cell V_{dc} as in (10),

$$k_{ijk}\left(\frac{NV_{dc}}{2}-\sqrt{\frac{3}{2}}V_g\right)\geq 0 \tag{9}$$

$$k_{ijk}\left(\frac{NV_{dc}}{2}+\sqrt{\frac{3}{2}}V_g\right)\leq V_{dc}\,, \tag{10}$$

Note that the third-order harmonic injection is utilized for the arm voltage v_{arm} as shown in Fig. 4. Therefore, the amplitude of the arm voltage v_{arm} in the simulation and the experimental verifications is 0.86 times smaller than the modulation method without the third-order harmonic injection. The (9) and (10) consider the third-harmonic voltage injection. Therefore, the maximum and the minimum value of the limitation of the coefficient k_{ijk} is derived from (9) and (10) by using the voltage redundancy ρ as,

$$0\leq k_{ijk}\leq\frac{4\rho}{N\left(\sqrt{3}+2\rho\right)}\,, \tag{11}$$

The limitation of the coefficient k_{ijk} is expressed by the number of cells in one arm N and the voltage redundancy ρ. The limitation of the imbalanced load is derived from (11) and (8) as in (12),

$$0\leq\frac{P_{cell,ijk}}{P_{arm,ij}/N}\leq\frac{4\rho}{\sqrt{3}+2\rho}\,, \tag{12}$$

The compensation capability for the load imbalance in one arm is expressed by only the voltage redundancy ρ. When all cells in one arm satisfy the limitation in (12), the cells in the arm operate without over-modulation. On the other hand, when any one of the cells does not satisfy the limitation in (12), the over-modulation occurs in that cell. As a result, the arm voltage $v_{arm,ij}$ distorts and the input current i_g have distortion. The limitation of the compensation capability of the proposed method is enlarged by the increase of the DC link voltage V_{dc}, as shown in (12).

Fig. 5 illustrates the limitation of the compensation capability resulting from (12). The voltage redundancy ρ is set to 1.22 in this paper. The horizontal and vertical axes in Fig. 5 indicate the load of a cell and the averaged load of the cells in one arm respectively, which are normalized to the rated output power of a cell. The red and blue dots in Fig. 5 indicate the maximum load in each arm of the multi-port converter for the simulation and the experimental verifications in the next chapter. The load imbalance is compensated by adjusting the coefficient k_{ijk} when all loads of cells are in the colored region in Fig. 5. On the other hand, the proposed method cannot compensate the load imbalance when the load imbalance of cells becomes large and the maximum load deviates from the colored region.

III. Simulation Result

Table I shows the simulation conditions. The voltage redundancy ρ is set to 1.22 in this paper. The maximum load imbalance between arms is 80%. The reactive component of the input current is set to zero in this simulation.

Fig. 6 shows the simulation results of the steady state operation with the proposed method. The maximum load of each

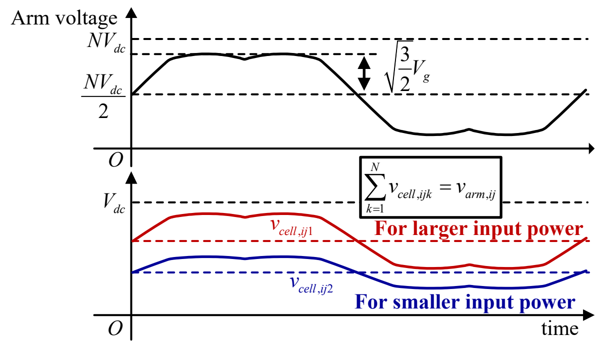


Fig. 4. Example of cell voltages with proposed divided voltage method in condition of larger output power of cell-j than that of cell-i.

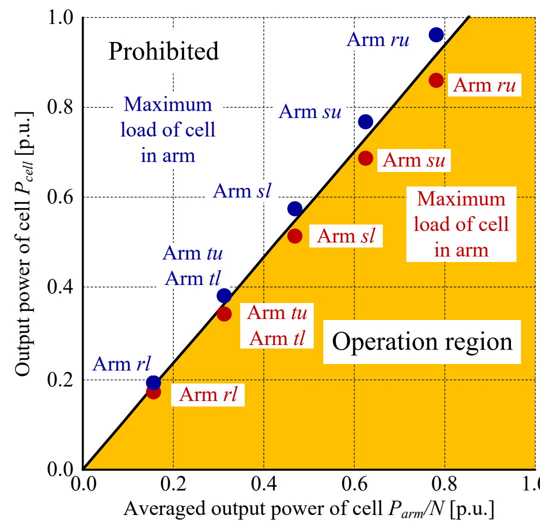
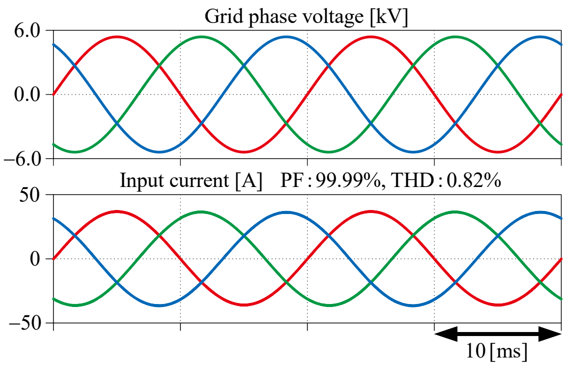


Fig. 5. Limitation of compensation capability of proposed divided voltage controller. The red dots indicates the maximum load in each arm for the simulation and experimental verification.

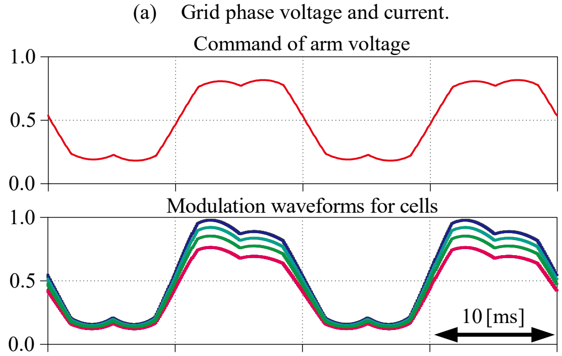
arm plotted on Fig. 5 as the red dots is set to satisfy the limitation shown in (12). The difference between the maximum and the minimum loads in one arm is set to 13% and 4 kind of load are used in this paper. The input current with the proposed method, as shown in Fig. 6 (a), is balanced and in-phase with the grid phase voltage. As an analysis result of the proposed method, the power factor (PF) of the input current is more than 99.99% and the THD of the input current is 0.82%. Fig. 6 (b) shows a command of the arm voltage and modulation waves for the cells in one arm with load imbalance. The amplitude of the modulation waves are differed in order to compensate the load imbalance in the proposed divided voltage controller. The modulation waves for cells are not scaled waveform from the command of the arm voltage. This is because the modulation waveforms for cells are obtained by dividing the output of the divided voltage controller by the DC link voltage of the cell including the voltage ripple. Fig. 6 (c) shows DC link voltage of all cells in the multi-port converter. The voltage error between the averaged DC link voltage of each cell and the command value of 264 V is about 2.1 V, which is less than 0.8%. Therefore, the proposed voltage divided controller is validated from these simulation results. Fig. 6 (d) shows the current flowing in the arms, which is the sum of the input current and the circulating current. The arm current shown in Fig. 6 (d) consists of the DC component and the grid frequency component. This is because

Table I Simulation condition.

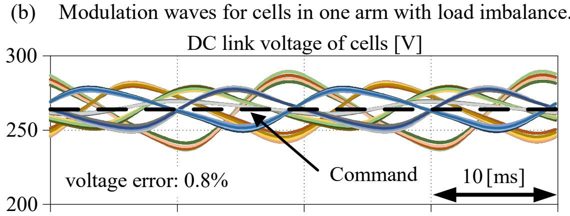
Parameter	Symbol	Value
Rated power of cell	P_{cell}	2.2 kW
Grid line-to-line voltage	$\sqrt{3}V_g$	6.6 kV (RMS)
Frequency of input voltage	f_g	50 Hz
Number of cells per arm	N	50
DC link voltage of cell	V_{dc}	264 V
Inductor	L	33 mH (0.16p.u.)
Capacitor	C	3.3 mF



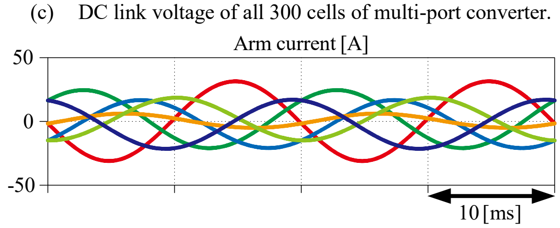
(a) Grid phase voltage and current.



(b) Modulation waves for cells in one arm with load imbalance.



(c) DC link voltage of all 300 cells of multi-port converter.



(d) Current flowing 6 arms

Fig. 6. Simulation result of steady-state operation under load imbalance. THD of the input current is 0.82% and PF is over 99.9%. The modulation waveforms for cells with larger output power becomes large and the DC link voltage for cells in one arm are converged to command with the error of 0.8% by the proposed controller.

the proposed divided voltage controller achieves the compensation of the load imbalance without any additional

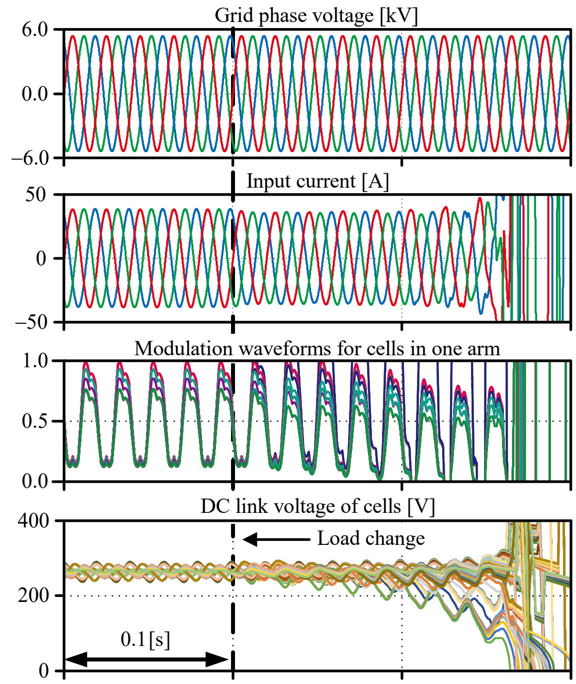


Fig. 7. Simulation waveform before and after load change. Before the load change, the load imbalance is compensated by the divided voltage controller because the load imbalance is within the limitation shown as red dots in Fig. 5. After the load change, the load imbalance becomes large and go out from the limitation as shown in blue dots in Fig. 5. The input current and DC link voltage gradually diverge.

circulating current for the compensation of the load imbalance in one arm.

Fig. 7 shows a transient behavior under load change. The load imbalance before the load change is within the limitation of the compensation capability shown as the red dots in Fig. 5. The load imbalance after the load change is out of the limitation of the compensation capability shown as the blue dots in Fig. 5. Before the load change, the maximum error of the averaged DC link voltage of cells are less than 0.1%. In addition, the input current is balanced and in-phase with the grid phase voltage. After the load change to the out of the limitation of the compensation capability, the amplitude of the modulation waveforms for cells with heavier load are increased according to (8) and over 1, i.e. over-modulation, as shown in Fig. 7. This over-modulation leads to insufficient of the input power to the cells. As a result, the DC link voltage imbalanced of the cells gradually expands as shown in the bottom of Fig. 7. In addition, the over-modulation of the cells results in distortion of the arm voltage and the current distorts, and the multi-port converter lose the control of the input current. The theoretical analysis is verified from this simulation results.

IV. Experimental Result

Fig. 8 shows the experimental setups. In addition, Table II shows the experimental conditions. A multi-port MMC prototype with 12 cells per arm was built in the laboratory. The maximum load imbalance between arms is 80%, which is the same as the simulation condition. The load imbalance in one arm plotted on Fig. 5 is set to only the upper arm of r-phase. The

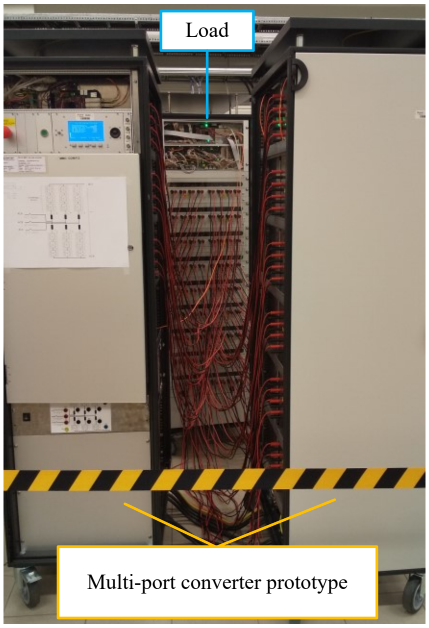


Fig. 8. The experimental setup of multi-port MMC prototype.

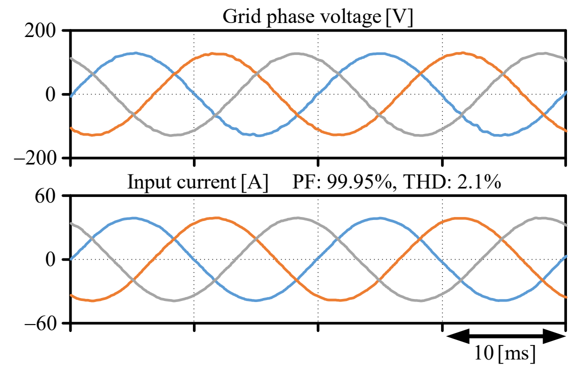
reactive component of the input current is set to zero in this experiment.

Fig. 9 depicts experimental waveforms of the steady state operation with the proposed method. The imbalanced of the loads in one arm is shown as the red dots in Fig. 5. The difference between the maximum and the minimum loads in one arm is set to 13%. In addition, the same load imbalance as the simulation condition are applied. As shown in Fig. 9 (a), the input current with the proposed method is balanced and in-phase with the grid phase voltage. As an analysis result of the proposed method, the PF of the input current is more than 99.9% and the THD of the input current is 2.1%. Fig. 9 (b) shows a command of the arm voltage and modulation waves for the cells in one arm with load imbalance. The amplitude of the modulation waves are differed in order to compensate the load imbalance. The modulation waveforms for cells are not scaled waveform from the command of the arm voltage. This is because the modulation waveforms for cells are obtained by dividing the output of the divided voltage controller by the DC link voltage of the cell including the voltage ripple. Fig. 9 (c) shows DC link voltage of cells in one arm. The voltage error between the averaged DC link voltage of each cell and the command value of 264 V is about 0.3 V, which is about 0.11%. The proposed voltage divided controller is validated from these simulation results. Fig. 9 (d) shows the current flowing 6 arms. The arm current shown in Fig. 9 (d) consists of the DC component and the grid frequency component. This is because the proposed divided voltage controller achieves the compensation of the load imbalance without any additional circulating current for the compensation of the load imbalance in one arm.

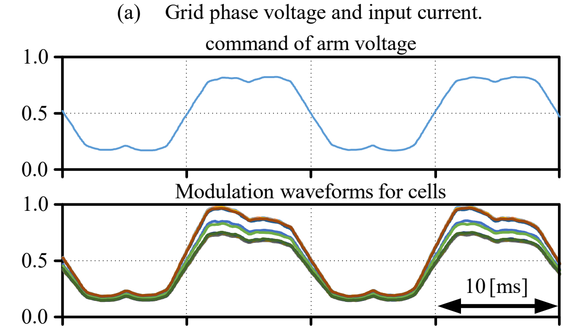
Fig. 10 shows a transient behavior under load change from 0.34p.u. to 0.86p.u. of one cell in upper arm of r-phase. The load imbalance before and after the load change is shown as red dots in Fig. 5 and the maximum load in one arm is not changed. After the load change, the DC link voltage of the cell with the load

TABLE II EXPERIMENTAL CONDITION.

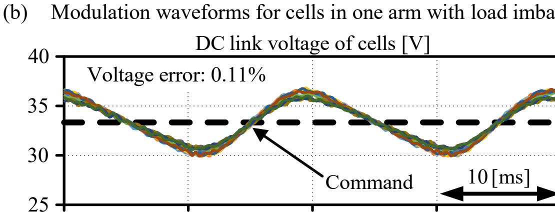
Parameter	Symbol	Value
Rated power of cell	P_{cell}	236 W
Grid line-to-line voltage	$\sqrt{3}V_g$	200 V (RMS)
Frequency of input voltage	f_g	50 Hz
Number of cells per arm	N	12
DC link voltage of cell	V_{dc}	33 V
Inductor	L	1.5 mH (0.20p.u.)
Capacitor	C	15 mF



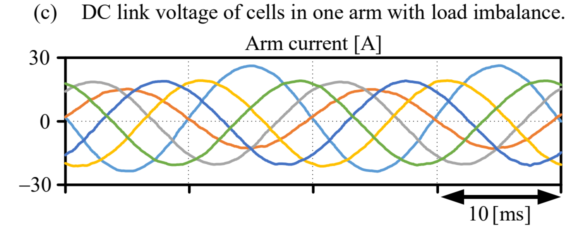
(a) Grid phase voltage and input current.



(b) Modulation waveforms for cells in one arm with load imbalance.



(c) DC link voltage of cells in one arm with load imbalance.



(d) Current flowing 6 arms.

Fig. 9. Experimental result of steady-state operation under load imbalance. THD of the input current is 1.9% and PF is over 99.9%. The modulation waveforms for cells with larger output power becomes large and the DC link voltage for cells in one arm are converged to command with the error of 0.8% by the proposed controller.

change decreases by about 16% at the maximum. Afterwards, the DC link voltage of the cell is converged to the command value of 33 V within 0.3 s. Fig. 10 (b) shows an enlarged waveform of the grid phase voltage, the input current, and the

DC link voltages of cells in the phase when load change occurs. No current distortion is observed when the load change.

V. Conclusion

This paper proposes the input current balancing method without any additional circulating current in the three-phase multi-port converter based on MMC in spite of the imbalanced load condition. In addition, the limitation of the proposed balancing control method was clarified for the load imbalance conditions. The validity of the theoretical analysis is verified by simulations. The experimental result showed the THD of the input current at grid side of 2.1% and the error of the DC link voltage of 0.11% thanks to the proposed control. In the future, the limitation of the compensation capability of the load imbalance in one arm will be enlarged by injecting higher harmonic components than DC and grid frequency component to the command of the cell voltage.

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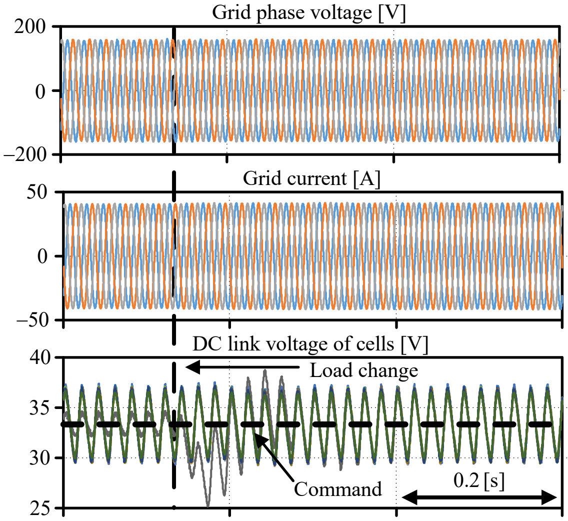
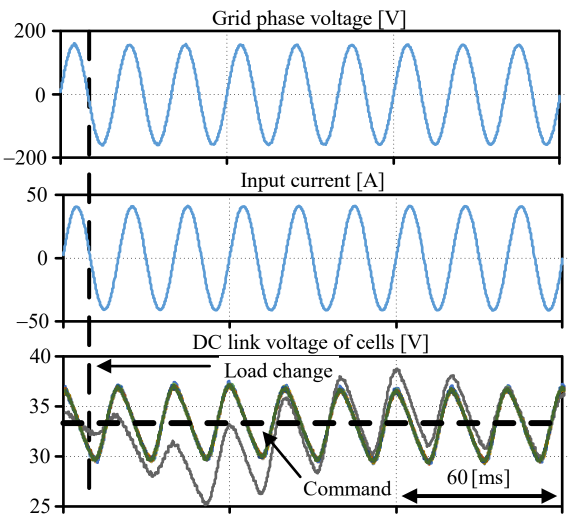


(a) Grid phase voltage, input current, and DC link voltage of cells in one arm whose load changed.



(b) Enlarged input current and DC link voltage of cells. The grid phase voltage and the input current shown in figure is only one phase whose load changed. Fluctuation of DC link voltage of 16% did not affect the input current.

Fig. 10. Transient response of proposed divided voltage controller under load change. The DC link voltages are converged to the command value within 0.3 s.

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