Current Balancing Method in Parallel Connected Inverter Circuit for Megahertz WPT System

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***Abstract*— This paper proposes a current balancing circuit of a parallel-connected inverter for a WPT system operated in megahertz. Current unbalance, which causes a thermal unbalance and deterioration of the devices, occurs at the output of each inverter when the output voltage has a difference between the inverters. Thus, the current balancing circuit, which is able to be applied for megahertz operation, is required. In this paper, the current balance circuit is investigated to achieve a parallel operation. The current balance circuit is composed of two transformers. A self-inductance ratio of the transformers, which is used in the balance circuit, is calculated by an analytical consideration to achieve the current balance condition. The proposed circuit is implemented into a prototype of the parallel-connected inverter operated around 6.78 MHz. From the experiments, it is demonstrated that the current unbalance of each inverter is 6.7% with the proposed balance circuit.**

Keywords—Current balance, Megahertz operation, Wireless power transfer, GaN-transistor

I. INTRODUCTION

In recent years, battery chargers for electric vehicles (EVs) are being developed rapidly by increasing the interest in EVs. Notably, wireless power transfer (WPT) systems for battery chargers have been actively studied for the viewpoint of safety and convenience in this decade [1–2]. Rapid charging is required for EVs to reduce the charging time because the charger using the WPT system takes a long time to charge the onboard batteries. Thus, increasing the output power of the WPT system to at least ten-kilo watts order output system is urgent.

WPT systems with a transmission frequency of 85 kHz have been commonly used in WPT systems. However, the ten-kilo watts order in the 85 kHz system is bulky and heavy because the WPT system has a ferrite in a transfer coil. A heavy system on the vehicle directly causes an increase in power consumption in the running. Thus, increasing the power density of the WPT system is necessary. Employing megahertz order switching frequency is one of the solutions to increase power density. Thus, the megahertz operation in a WPT system has been actively studied [3–8].

Inverter circuit, which is applied to WPT system in megahertz operation, requires nano-second order switching. Thus, a GaN device, which can switch in a few nano-second, is applied for the WPT system [9–10]. However, the output power is regulated in a few kilo-watts because the rated power of the GaN device is still low. On the other hand, the output power of the WPT system requires ten-kilowatt order to achieve rapid charging for EVs. Thus, a parallel connection of the GaN devices or inverter circuits [11–12] is necessary to accomplish a ten-kilo watts order system. Then, the current balancing method is required to achieve the parallel connection because the output voltage has a difference due to the delay of the switching timing and the difference of the parasitic parameters of the devices between the inverters. Current unbalance causes thermal unbalance, which may cause the brake of the devices. However, the difficulty of the accurate control of a switching timing is still a serious problem because the control period should be smaller than a few nano-second in megahertz operation. Moreover, the accurate adjusting of parasitic parameters is also difficult. Thus, the current balancing method should be employed by passive components without additional current control.

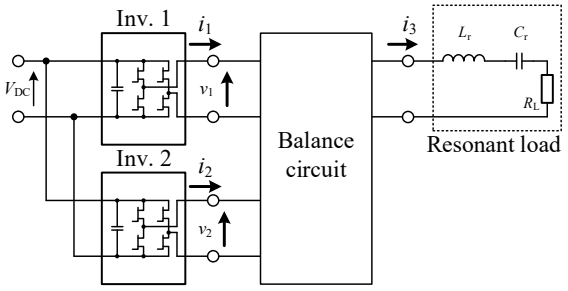

Fig. 1. Configuration of the balance circuit in parallel-connected inverter system.

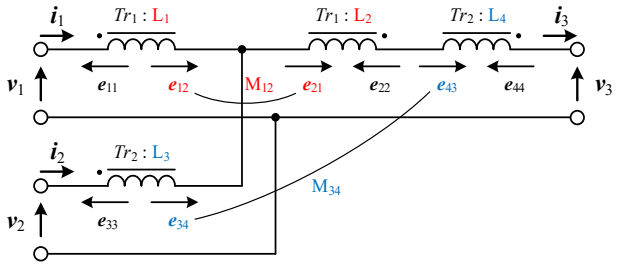

Fig. 2. Configuration and induced voltage in balance circuit.

In this paper, the current balancing method is studied for parallel-connected inverters in megahertz operation. The advantage of the proposed method is that only passive components are required because it is hard to control the megahertz operation system with nano-second order of control time. The rest of this paper is organized as follows. First, a balancing circuit is theoretically analyzed. The balancing circuit is composed of two transformers to achieve the balancing operation in a parallel structure. Then, the working of the balancing circuit is simulated in the megahertz operation. Finally, a prototype with the proposed balance circuit is demonstrated.

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II. CURRENT BALANCING METHOD

A. Configuration of Current Balance Circuit

Parallel connection of the megahertz inverter circuit is necessary to achieve high output power in a WPT system. However, the current unbalance occurs between paralleled circuits caused by the phase difference or the output voltage difference of each circuit. Thus, the balance circuit, which absorbs the difference of output voltage in each inverter, is necessary. Figure 1 shows the structure of the parallel-connected inverter using the balance circuit for the WPT system. The balance circuit is connected to the outputs of the inverters. The resonant circuit is connected to the output side of the balance circuit as a load.

Figure 2 shows the configuration and induced voltage of the current balance circuit. The balance circuit consists of two transformers. The primary side of each transformer is connected to the output of each inverter. The secondary side of each transformer is connected to a resonant load in series.

B. Design of Inductance Ratio of Transformer in Balancer

The output voltage $\boldsymbol{v}_1$ of the inverter is given by

$$\boldsymbol{v}_1 = \boldsymbol{e}_{11} - \boldsymbol{e}_{12} + \boldsymbol{e}_{22} - \boldsymbol{e}_{21} + \boldsymbol{e}_{44} - \boldsymbol{e}_{43} + \boldsymbol{v}_3 \quad \text{..... (1).}$$

In the balance circuit, currents $\boldsymbol{i}_1$, $\boldsymbol{i}_2$, and $\boldsymbol{i}_3$ are sinusoidal because the resonant load is applied. Thus, $\boldsymbol{v}_1$ is expressed as

$$\boldsymbol{v}_1 = j\omega\left(L_1 - M_{12}\right)\boldsymbol{i}_1 + j\omega\left(L_2 - M_{12} + L_4\right)\boldsymbol{i}_3 - j\omega M_{34}\boldsymbol{i}_2 + \boldsymbol{v}_3$$
$$\text{..... (2),}$$

where L_1, L_2, L_3, and L_4 are the self-inductances of each wiring, M_{12} and M_{34} are the mutual-inductance. When two transformers have the same self-inductance and mutual-inductance, each inductance is expressed as

$$L_1 = L_3 = L_{pri} \quad \text{..... (3),}$$
$$L_2 = L_4 = L_{\mathrm{sec}} \quad \text{..... (4),}$$
$$M_{12} = M_{34} = M \quad \text{..... (5),}$$

where the L_{pri} represents the self-inductance of the primary side, L_{sec} represents the self-inductance of the secondary side, M represents mutual inductance. Equation (2) is simplified as

$$\boldsymbol{v}_1 = j\omega\left(L_{pri} - M\right)\boldsymbol{i}_1 + j\omega\left(2L_{\mathrm{sec}} - M\right)\boldsymbol{i}_3 - j\omega M\boldsymbol{i}_2 + \boldsymbol{v}_3$$
$$\text{..... (6).}$$

Similarly, the output voltage $\boldsymbol{v}_2$ is also expressed as

$$\boldsymbol{v}_2 = j\omega\left(L_{pri} - M\right)\boldsymbol{i}_2 + j\omega\left(2L_{\mathrm{sec}} - M\right)\boldsymbol{i}_3 - j\omega M\boldsymbol{i}_1 + \boldsymbol{v}_3$$
$$\text{..... (7).}$$

Then (6) is added to (7),

$$\boldsymbol{v}_1 + \boldsymbol{v}_2 - 2\boldsymbol{v}_3 = j\omega\left(L_{pri} - 2M\right)\left(\boldsymbol{i}_1 + \boldsymbol{i}_2\right) + 2j\omega\left(2L_{\mathrm{sec}} - M\right)\boldsymbol{i}_3$$
$$\text{..... (8).}$$

When the ideal current balancing is achieved, the output voltage $\boldsymbol{v}_3$ is the average value of each input voltage $\boldsymbol{v}_1$ and $\boldsymbol{v}_2$. Furthermore, each input current $\boldsymbol{i}_1$ and $\boldsymbol{i}_2$ is the same value, and the output current $\boldsymbol{i}_3$ is two times larger than each input current. Each voltage and current condition in ideal balancing condition is expressed as

$$\boldsymbol{v}_3 = \frac{\boldsymbol{v}_1 + \boldsymbol{v}_2}{2} \quad \text{..... (9),}$$

$$\boldsymbol{i}_1 = \boldsymbol{i}_2 = \frac{\boldsymbol{i}_3}{2} \quad \text{..... (10).}$$

Then, (9) and (10) are applied to (8), inductance equation in the current balance condition is expressed as

TABLE I. Simulation parameter.

Main circuit parameter		
DC link voltage	V_{DC}	300 V
Rated power of each inverter	P	2 kW
Switching frequency	F_{s}	6.78 MHz
Duty	d	40%
Parasitic capasitance at drain-source of GaN-Transistor	C_{ds}	127 pF
Balancer paameters		
Inductance of primary side	L_{pri}	5.7 μH
Inductance of secondary side	L_{sec}	1.425 μH
Load parameters		
Resonant inductance	L_{r}	5.7 μH
Resonant capacitance	C_{r}	100 pF
Load resistance	R_{L}	10 Ω

$$L_{pri} - 4M + 4L_{\mathrm{sec}} = 0 \quad \text{..... (11).}$$

Mutual inductance M is expressed as

$$M = k\sqrt{L_{pri}L_{\mathrm{sec}}} \quad \text{..... (12),}$$
$$k = 1 \quad \text{..... (13),}$$

where k is the coupling coefficient, which is considered as unity in an ideal condition. Using (11), (12), and (13), the relationship of L_{pri} and L_{sec} in balancing condition is expressed as

$$L_{pri} = 4L_{\mathrm{sec}} \quad \text{..... (14).}$$

As a result, the winding ratio of the primary windings to the secondary windings is 2:1 to achieve the balancing condition of the output current of each inverter.

C. Influence of Leakage Inductance in Balancer

Resonant inductance and capacitance are essential factors to transmit the power in the WPT system. Thus, the leakage inductance at the transformer should be considered to satisfy the resonant conditions. The voltage equation between the output voltage of Inv. 1 v_1 and output voltage of the balance circuit v_3 is expressed as

$$\boldsymbol{v}_1 - \boldsymbol{v}_3 = j\omega\left(L_{pri} - M\right)\boldsymbol{i}_1 + j\omega\left(2L_{\mathrm{sec}} - M\right)\boldsymbol{i}_3 - j\omega M\boldsymbol{i}_2$$
$$\text{..... (15).}$$

Then, the current balancing condition (10) is applied to (15),

$$\boldsymbol{v}_1 - \boldsymbol{v}_3 = j\omega\left(\frac{L_{pri}}{2} - \frac{M}{2} + 2L_{\mathrm{sec}} - M - \frac{M}{2}\right)\boldsymbol{i}_3 \quad \text{..... (16).}$$

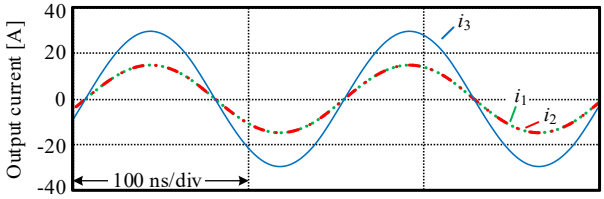
Similarly, the voltage equation between the output voltage of Inv. 2 v_2 and output voltage of the balance circuit v_3 is also expressed as

$$\boldsymbol{v}_2 - \boldsymbol{v}_3 = j\omega\left(\frac{L_{pri}}{2} - \frac{M}{2} + 2L_{\mathrm{sec}} - M - \frac{M}{2}\right)\boldsymbol{i}_3 \quad \text{..... (17).}$$

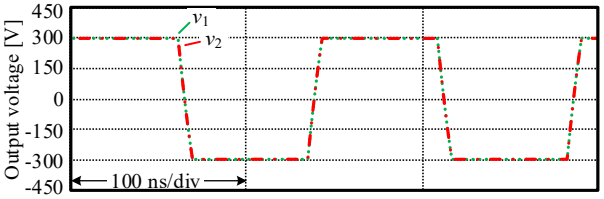
Inductance between the output of each inverter and output of the balance circuit is expressed as

$$L_{\mathrm{balancer}} = \frac{L_{pri}}{2} - \frac{M}{2} + 2L_{\mathrm{sec}} - M - \frac{M}{2} \quad \text{..... (18),}$$

where L_{balancer} represents the inductance from the output of each inverter to the output of the balance circuit. Equation (18) is derived as

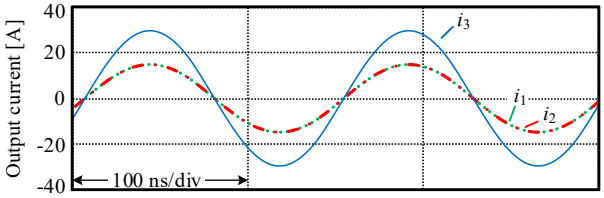


(a)Output current.

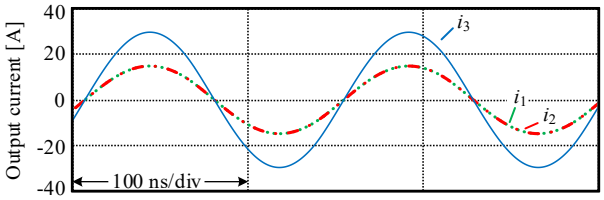


(b)Output voltage.

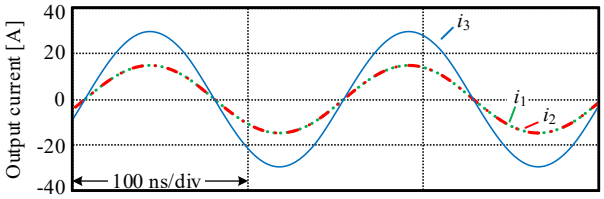
Fig. 3. Output voltage and current in ideal condition.



(a)Coupling coefficient k : 0.9.

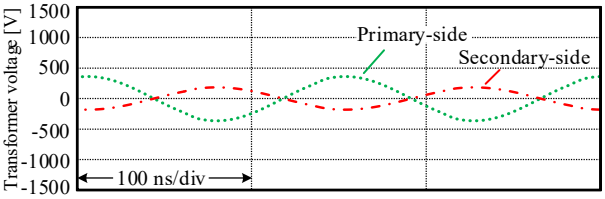


(b)Coupling coefficient k : 0.8.

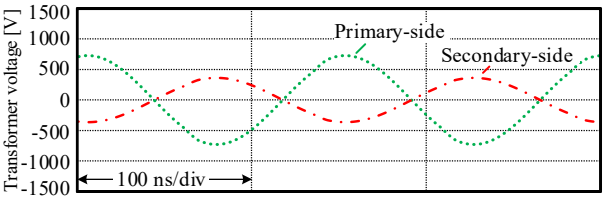


(c)Coupling coefficient k : 0.7.

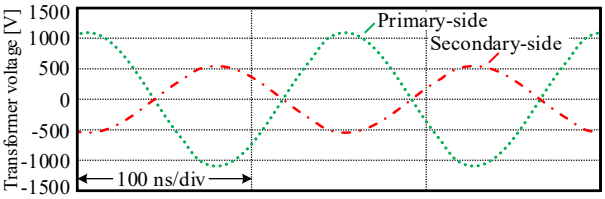
Fig. 4. Output current with variation of coupling coefficient.



(a)Coupling coefficient k : 0.9.



(b)Coupling coefficient k : 0.8.



(c)Coupling coefficient k : 0.7.

Fig. 5. Winding voltage at Tr_1 with variation of coupling coefficient.

$$L_{balancer} = 4L_{sec}(1-k) \quad \text{..... (19),}$$

by applying (12), (13), and (14) to the (18). The influence of the leakage inductance appears in (19). Thus, $L_{balancer}$ should be compensated to satisfy the resonant condition.

III. Simulation Result

The current balancing in a parallel-connected inverters circuit is verified by simulation. The rated power of each inverter is 2 kW, the total output power is 4 kW. Table I shows the simulation parameters. The self-inductance of the primary winding L_{pri} is determined to be the same value as resonance inductance.

A. Zero Leakage Inductance Condition

Figure 3 shows the output voltage and current in ideal condition. There is no difference in the output voltage between the two inverters, and the coupling coefficient k is 1.0. The output current of each inverter is completely balanced in the ideal conditions.

B. Leakage Inductance Condition

Figure 4 shows the current waveforms when k is changed from 0.7 to 0.9. The resonant condition does not change because the leakage inductance of the balancer is compensated by adjusting resonant inductance L_r based on (19). The current balancing is also achieved with the difference of the coupling coefficient. Figure 5 shows the voltage waveform of the transformer with the variation of the coupling coefficient. The voltage of the transformer increases with decreasing the coupling coefficient.

C. Phase Delay of Output Voltage in Inv. 2 with Zero Leakage Inductance

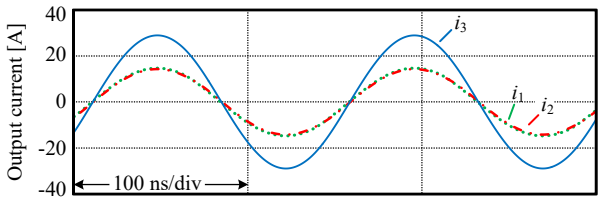
Current balancing is simulated with a phase difference of the output voltage between two inverters. The phase of the output voltage in the Inv. 2 is purposely delayed from Inv. 1 by 5%, 10%, and 25% of the time period. The coupling coefficient k is 1.0.

Figure 6 shows the output current with phase delayed condition. Total output current decreases gradually as the increasing of phase delay value. The output current of each inverter is almost balanced in a 5% delayed condition. However, a slight difference in the output current occurs with 10% and 25% delayed conditions. Figure 7 shows the output voltage with phase delayed condition. A zero-voltage switching (ZVS) is not achieved at Inv. 2 with 10% and 25% delayed condition.

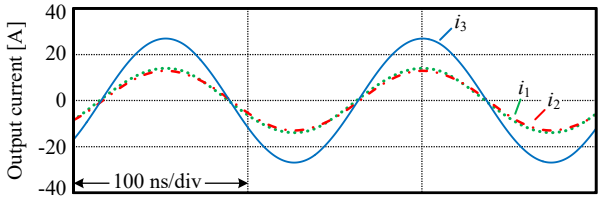
D. Variation of Voltage Amplitude in Inv. 2 with Zero Leakage Inductance

Current balance working is simulated with the difference of the amplitude of the output voltage between two inverters. The maximum output voltage of Inv. 2 is decreased to 290 V, 150 V, and 0 V. The maximum output voltage of Inv. 1 is 300 V in any condition. The phase delay value is zero and coupling coefficient k is 1.0.

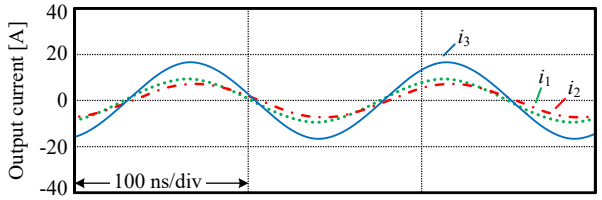
Figure 8 shows the output current with voltage difference condition. The output current balances in any voltage condition. Furthermore, the total output current i_3 in the



(a)Phase delay : 5% (7.4 ns).

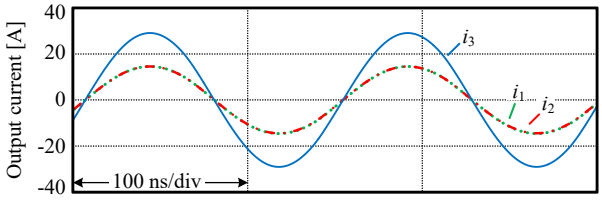


(b)Phase delay : 10% (14.7 ns).

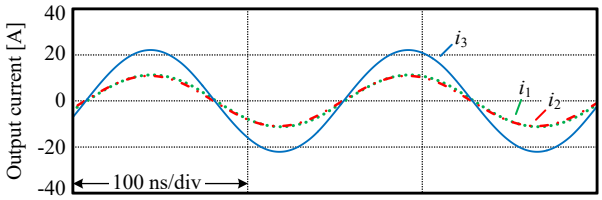


(c)Phase delay : 25% (36.9 ns).

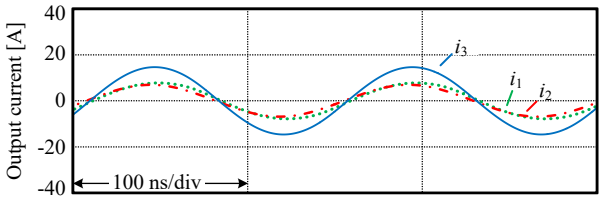
Fig. 6. Output current with phase delay.



(a)Voltage difference : 10 V



(b)Voltage difference : 150 V

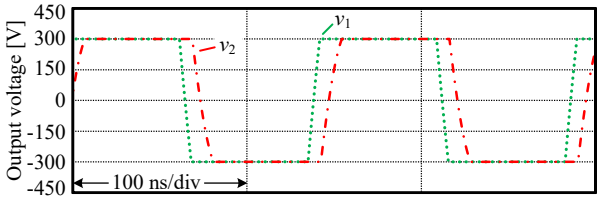


(c)Voltage difference : 300 V

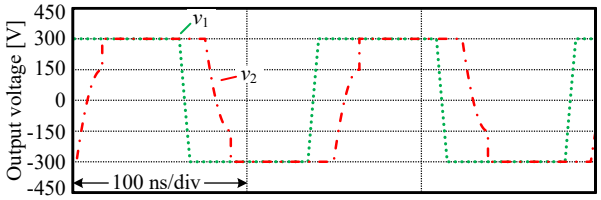
Fig. 8. Output current with voltage difference.

condition of $v_2 = 0$ is the half value of the ideal condition. Figure 9 shows the output voltage with voltage difference condition. The ZVS is achieved in any voltage condition.

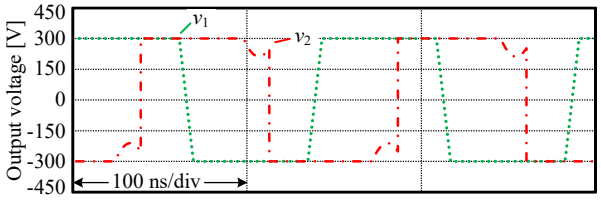
The result with voltage difference condition indicates that the total output current of the balance circuit i_3 is proportional to the average of each output voltage. Moreover, the output current keeps conduction when the inverter does not output the voltage as shown in figure 9 (c). The current should be convection even if some devices are broken. Thus, an additional current pass such as a diode is required.



(a)Phase delay : 5% (7.4 ns).

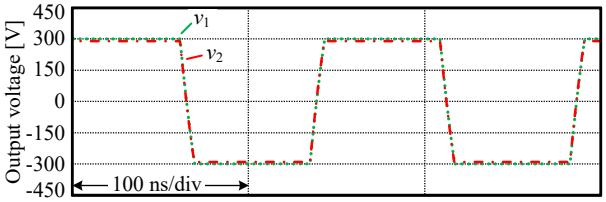


(b)Phase delay : 10% (14.7 ns).

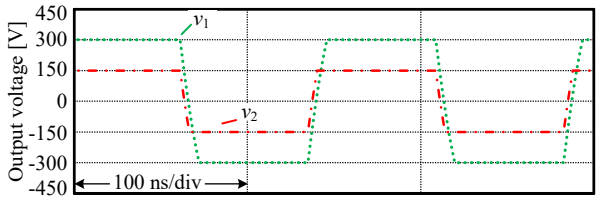


(c)Phase delay : 25% (36.9 ns).

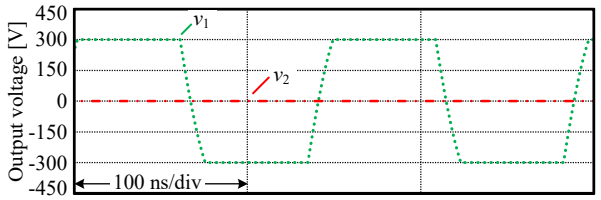
Fig. 7. Output voltage with phase delay.



(a)Voltage difference : 10 V



(b)Voltage difference : 150 V

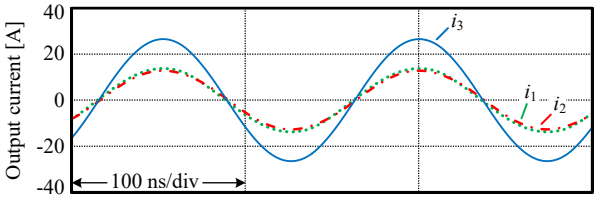


(c)Voltage difference : 300 V

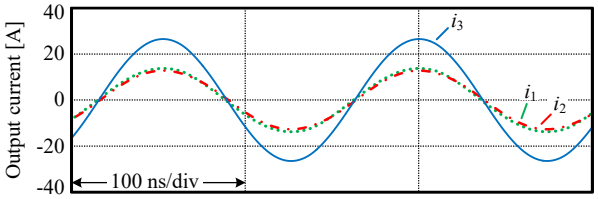
Fig. 9. Output voltage with voltage difference.

E. Phase Delay and Variation of Voltage Amplitude in Inv.2 with Leakage Inductance

This section shows a simulation result with the variations of the phase and amplitude of the output voltage when the coupling coefficient is not unity. The phase delay is caused by a length difference of signal lines or dispersion of delays in ICs and switching devices in an experiment. The phase difference is selected to the 10% of the time period by considering the above differences. The difference in the voltage amplitude is caused by a difference of parasitic parameters of the devices, printed circuit boards, and a dispersion of the on-resistance at the devices in an experiment. Thus, the maximum output voltage of Inv. 2 is selected to 290

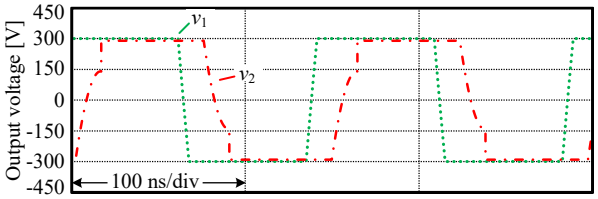


(a)Coupling coefficient k : 0.9.

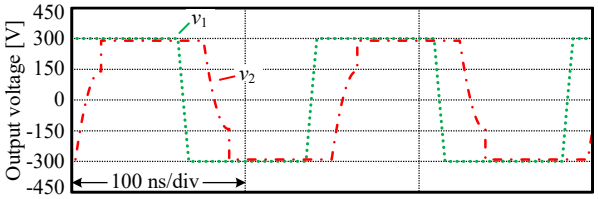


(b)Coupling coefficient k : 0.7.

Fig. 10. Output current with variations of phase and amplitude.

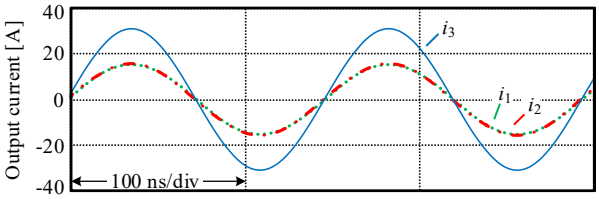


(a)Coupling coefficient k : 0.9.

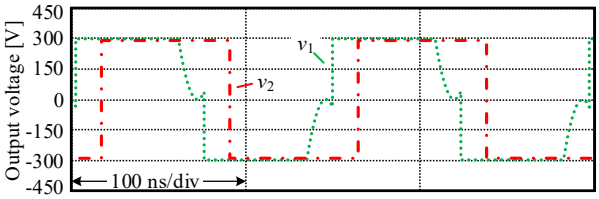


(b)Coupling coefficient k : 0.7.

Fig. 11. Output voltage with variations of phase and amplitude.

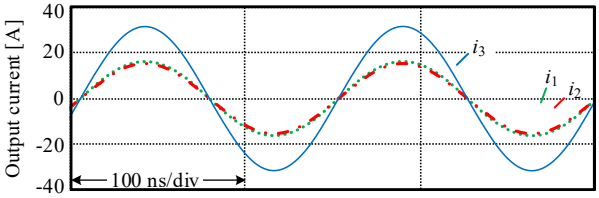


(a)Output current.

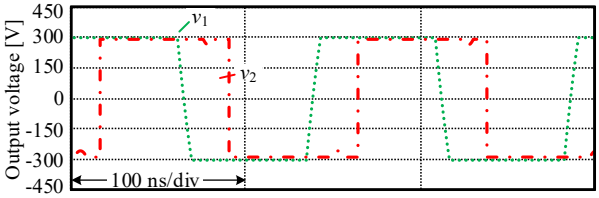


(b)Output voltage.

Fig. 12. Output current and voltage with self-inductance difference between Tr1 and Tr2.



(a)Output current.



(b)Output voltage.

Fig. 13. Output current and voltage with difference of the ratio of self-inductance.

V due to the difference of the parasitic parameters. The coupling coefficient k is 0.7 and 0.9.

Figure 10 shows the current waveforms with the variations of the phase and amplitude of the output voltage. The current balancing is also achieved. Figure 11 shows the output voltage waveforms. ZVS is achieved in Inv. 1, whereas ZVS is not achieved in Inv. 2.

F. Variation of Self-inductance in Balance Circuit

The self-inductance of two transformers, which are used in balancer, has tolerance in a prototype. Moreover, a ratio of the inductance at the primary-side and secondary-side also has a slight difference from the designed value. Thus, the working of the current balancing with the inductance variation is necessary. The maximum output voltage of Inv. 2 is 290 V, the phase delay of the output voltage of Inv. 2 is 5% from Inv. 1, and the coupling coefficient k is 0.8 in the following simulation.

Figure 12 shows the output current and voltage of the inverter with a variation of the self-inductance between the two transformers. The self-inductances of the Tr_1, L_1 and L_2, are 1.5 times as much as the self-inductance of the Tr_2, L_3 and L_4. From figure 12(a), the current balance is achieved between two inverters. However, the ZVS working at the output voltage of each inverter is not achieved, as shown in figure 12(b).

Figure 13 shows the output current and voltage of two inverters with a difference in the ratio of the self-inductance at

TABLE II. Parameters of experimental circuit.

Main circuit parameter		
DC link voltage	V_{DC}	200 V
Switching frequency	F_s	6.4 MHz
Duty	d	36%
Balancer paameters		
Inductance of primary side	L_{pri}	4.3 µH
Inductance of secondary side	L_{sec}	1.3 µH
Coupling factor	k	0.84
Load parameters		
Resonant inductance	L_r	5.7 µH
Resonant capacitance	C_r	100 pF
Load resistance	R_L	10 Ω

the primary-side and secondary-side. The self-inductance of the primary-side L_1 and L_3 is 1.5 times as much as the designed value. As a result, the inductance ratio of the primary-side to the secondary-side is 6:1. From figure 13(a), the current balance is also achieved between two inverters. However, the ZVS working of the output voltage of Inv. 2 v_2 is not achieved, as shown in figure 13(b).

IV. Experiments of Current Balancing

The current balancing with the proposed balancer is demonstrated with the parallel-connected inverters. Table II shows the circuit parameters for the experiment. Figure 14

shows the balance circuit. The transformer used in the balancer has no core. Moreover, the two transformers are orthogonalized to avoid magnetic interference.

A. Current Balancing without Phase Delay

Figure 15 shows the output current and voltage without phase delay. The amplitude of output voltage has a difference of about 20 V. The output current of each inverter is balanced with the difference of output voltage. Moreover, The output voltage of each inverter achieves the ZVS.

B. Current Balancing with Phase Delay

Figure 16 shows the output current and voltage with a phase delay. The output voltage of Inv. 2 delayed 5.7 ns (3.8%) from Inv. 1. The output current of each inverter is almost balanced. The maximum current of Inv.1 i_{inv1} is 4.5A and the maximum current of Inv.2 i_{inv2} is 4.2A. The error rate of the output current is about 6.7%. The output voltage of each inverter achieves the ZVS working.

V. Conclusion

In this paper, the current balance circuit for a parallel-connected inverter in the megahertz operation has been proposed. The proposed circuit employs only passive components, which do not need any additional current control. The balancing circuit consists of two transformers. The ratio of the self-inductance of the transformers, primary-side to secondary-side, to achieve the current balancing is derived from the voltage equations. The current balance working is simulated with the phase difference and amplitude difference of the output voltage between two inverters. Each output current is balanced with the phase difference and amplitude difference of the output voltage, and the self-inductance difference of the balance circuit. Further consideration of the ZVS condition of each inverter is necessary. The proposed balance circuit is implemented into a prototype of the parallel-connected inverter circuit. From the experiments, it is demonstrated that the output current of each inverter is balanced with an error rate of 6.7% when the 3.8% phase delay and 20V amplitude difference between the two inverters in megahertz operation.

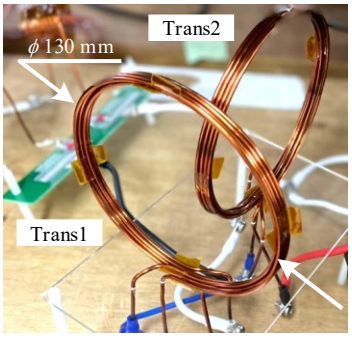


Fig. 14. Balance circuit at 6.78 MHz range.

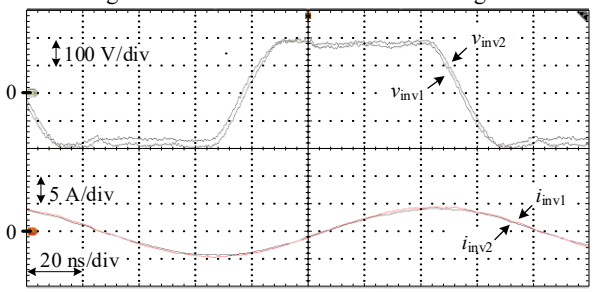


Fig. 15. Output voltage and current without phase delay.

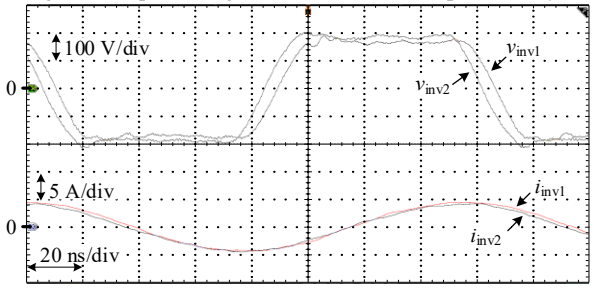


Fig. 16. Output voltage and current with 5.7 ns(3.8%) phase delay.

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