Droop-based Current Control Method in Autonomous Distributed Modular Power Conversion System

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***Abstract*— This paper proposes a decoupling control method among autonomous distributed modular power modules for an Universal Smart Power Module (USPM) concept. In this concept, the power conversion systems are configured as the Power Electronics Building Block (PEBB) to realize the simplification of the power electronics design. The original point of USPM is that each power module operates independently because a high-speed power electronics controller is implemented on each power module. The power modules of PEBB are typically configured by the main power circuits with gate controllers. Therefore, the controller is designed specifically according to various applications although the advantages of PEBB are high flexibility and user-friendly. USPM enhances these advantages in comparison with the PEBB. The USPM systems establish a decoupling method among each USPM because USPM does not share the physical information among the other USPMs. In addition, USPM is utilized in the multi-series and parallel connection to increase the voltage and current rating of the power system according to the applications. In this paper, a droop-based current control for series connection USPM is proposed in order to stabilize the current control of each USPM. Furthermore, the design criteria of the droop control are revealed. The experimental result with series-connected USPMs demonstrate that the proposed method avoided the overmodulation due to interference of the current controllers of each USPM. In addition, the current deviation in the experiment was coincident with the current deviation in design with an error of 3.17%.**

Keywords—droop control, autonomous decentralized control, Universal smart power module

I. INTRODUCTION

Power conversion systems based on the modular structure such as the PEBB concept have been widely considered in order to realize high system reliability and high system extensibility [1-6] for UPS, microgrids, and etc. Basic idea of these power modules is that the power module units are stacked depending on the requirement of the voltage and current rating in the larger scale power conversion systems than one power module. The PEBB concept is expected to improve productivity due to cost reduction and shorter development period because the developer is not required to produce the module with different rating. In addition, PEBB has high reliability in that it is repaired by exchanging only a defective module during maintenance. In particular, the high productivity of the modular structure would become important in future power electronics systems because the demand of the power conversion systems drastically increases owing to increase of electric energy, e.g. Electric Vehicle (EV) and renewable energy sources. PEBBs integrate the switching devices, passive components, and some auxiliary circuit in the power conversion unit. Note that the conventional PEBB system requires the central controller in order to regulate each PEBB. In addition, the input/output filter is not included in PEBBs. Development of them requires complicated and diverse know-how as well as the conventional power conversion system [7-10] development. Thus, PEBB concept still challenges of high development costs and long development times because it is not sufficient as the building blocking of the power conversion systems.

In this paper, a novel Universal Smart Power Module (USPM) concept is proposed. USPM realizes user-friendly design and high scalability compared to PEBB because USPM is designed to be generic. USPM realize driving with only one USPM and various power conversions by multiple distributed USPMs because the USPM includes all power conversion elements such as the high-speed controller and the main circuit. In addition, the droop-based current control and its design method are also proposed in order to stabilize the operation of each distributed USPM. The voltage droop control for the parallel connection of the voltage sources has been proposed in many studies [10-15]. On the other hand, the series operation of the current sources has not been studied because there was no application using the current source modules in series. The proposed method is realized by using duality for the voltage droop control. The design method of the current droop control is easily designed with the gain characteristics of the current droop control in formula.

The configuration of this paper is as follows. Chapter 2 explains the outline and the control of the USPM concept.

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Chapter 3 proposes the current droop control applied to series connection of modules based on the duality of the voltage droop control. Chapter 4 expounds the gain design method of the current droop control for the series modules with the wide compensation range. Chapter 5 demonstrates the simulation and the experiment with the designed the current droop gain. As a result, the stable operations thanks to the designed gain were confirmed. In addition, the current deviation in the experiment was coincided with 3.17% for the design value.

II. PEBB AND UNIVERSAL SMART POWER MODULE (USPM)

Figure 1 shows the configuration of the power conversion systems based on the PEBB concept [16]. In this system, the main circuit and the gate drive unit are configured as the modular based configuration while the auxiliary circuit and the controller are

designed corresponding to the various applications. PEBB has advantages, e.g., the low cost, high reliability, high extensibility, easy to use, and easy to maintenance. However, the conventional PEBB is not fully building-blocked because the system controller and the auxiliary circuit such as the detection circuit have to developed as well as the conventional power conversion system. Therefore, the power converter design by PEBBs is still complex, and a lot of know-how is necessary. In order to solve this problems, the USPM concept is proposed in this paper.

Figure 2 shows the USPM system. The difference between USPM and PEBB is that USPM has the input/output filter, the high-speed slave controller, and wire-less communications between the master and the slave controller. The master controller regulates all USPMs, and it gives the information such as the voltage or current command to each USPM. USPM generates the required voltage or current waveforms because it has high responsiveness owing to into the high-speed slave controller.

USPM has high modularity and expandability because each USPM behave as the one of the power converter independently. In addition, this system is configured only with master controller and USPM. Therefore, the circuit design is drastically simplified in comparison with the conventional power converter and PEBB. Furthermore, the various power conversions such as AC to AC and DC to DC in the power converters with USPMs and the flexible design of the power rating by changing the number of USPMs bring the high usability and the high scalability to the power converter design.

Figure 3 shows an example of single-phase AC-AC power conversion system with USPM. The primary side USPM controls the grid current, and the secondary side USPM controls the load voltage. The main power circuit of USPM consists of the H-bridge converter including the LCL filter for usability and versatility. An isolated DCDC converter is connected between primary side USPM and secondly side USPM to prevent short circuit. In this system, the sinusoidal input current waveforms is obtained as the PFC converter, and the voltage rating of the system is extended by increasing the number of series connected USPMs. In addition, each USPM contains an decentralized high-speed controller to control the input / output voltage or current of USPM. Note that some

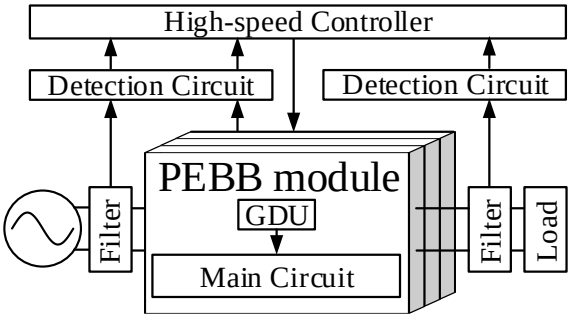


Figure 1. Power conversion system applying PEBB concept. PEBB system requires special design of filters and controllers separately from modules.

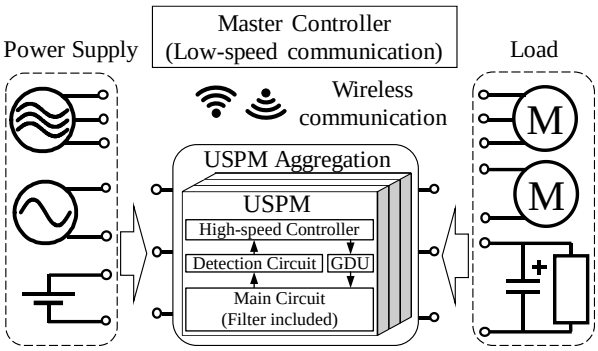


Figure 2. Power conversion system with USPM. Various applications are applied by transmitting command to USPM with wireless communication.

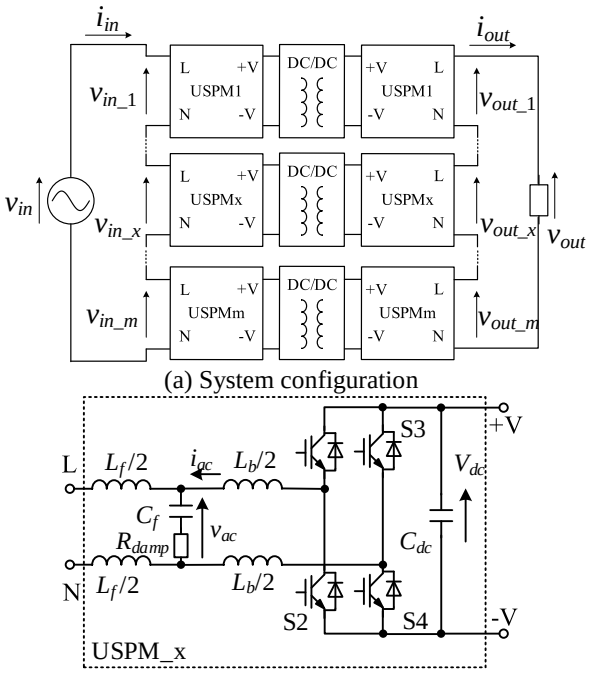


Figure 3. Single-phase AC-AC power conversion system with USPM. USPM has an H-bridge configuration that includes an LCL filter.

internal information such as the instantaneous current value is not shared among the high-speed controllers of each USPM in order to simplify the system configuration. As a result, the primary side USPM current detection delay or detection gain imbalance caused by the temperature drift of the current sensor will interfere with the current control. Therefore, the stabilization technique is required for each USPM controller. Note that the stabilization method does not requires the high-speed communication between the master and the slave controller.

III. Proposed Current Droop Control

The droop control is a non-interference control with excellent modularity that does not require to share information such as voltage and current between modules. The droop control is very compatible with the concept of USPM in which some information is not shared among modules. Therefore, the droop control is adopted as the non-interference control of the series-connected controlled current source. Note that, in this paper, a DC power supply is connected to the primary DC link in order to verify the current droop control.

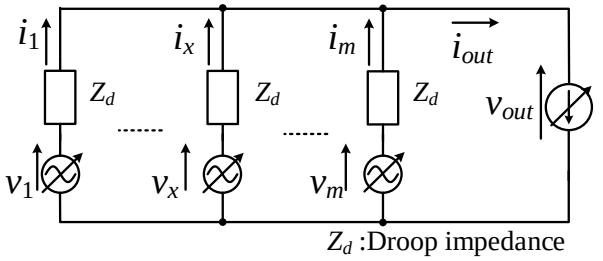
Figure 4(a) shows the equivalent circuit of the voltage droop control, where the voltage sources v_1, v_x, and v_m are the voltages output by each voltage source module, v_{out} and i_{out} are the output voltage and the output current applied to the load. In addition, the subscript x in the voltage source indicates an x-th module of the parallel-connected voltage source modules, and the subscript m indicates the number of modules of the parallel-connected voltage source modules. Note that each module operates as an ideal voltage source because it controls the voltage independently. The voltage droop control suppresses the interference of the voltage sources connected in parallel by providing the controlled voltage source a drooping characteristic. The voltage droop control is achieved by connecting a virtual droop impedance Z_d in series to voltage sources. The voltage droop control has the characteristic that the output voltage v_{out} drops due to the voltage drop caused by Z_d.

Figure 4(b) shows the equivalent circuit of the current droop control where the current sources i_1, i_x, and i_m are the currents output by each current source module, v_{ac} is the grid voltage, and i_{ac} is the current flowing into the grid. In addition, the subscript x in the current source indicates any module in the series-connected current source module, and the subscript m indicates the number of modules in the series-connected current source module. Note that each module operates as an ideal current source, since current control is applied independently to each module. The current droop control is considered as the duality of voltage droop theory. Therefore, the current droop control suppresses the interference of the current sources connected in series by connecting a virtual droop admittance Y_d in parallel to the current sources. The current droop control is obtained by subtracting the droop current from the current command. The droop current is given by;

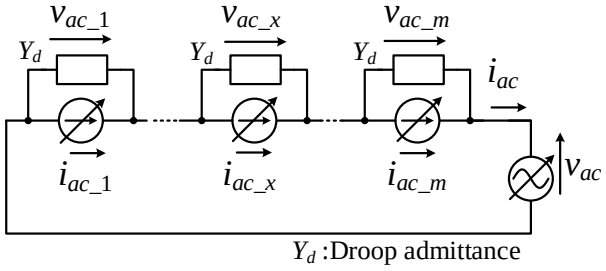
$$i_{ac} = \frac{\sum_{y=1}^{m} i_y}{m + Y_{d\_p.u.}} \tag{1}$$

where, $Y_{d\_p.u.}$ is the virtual resistance Y_d standardized by the rated admittance Y_n of each module.

Figure 5 shows the control block diagram of the USPM.



(a) Voltage droop control



(b) Current droop control

Figure 4. Equivalent circuit of droop control. The droop control suppresses control interference by inserting a virtual impedance. The current droop control has a duality with the voltage droop control.

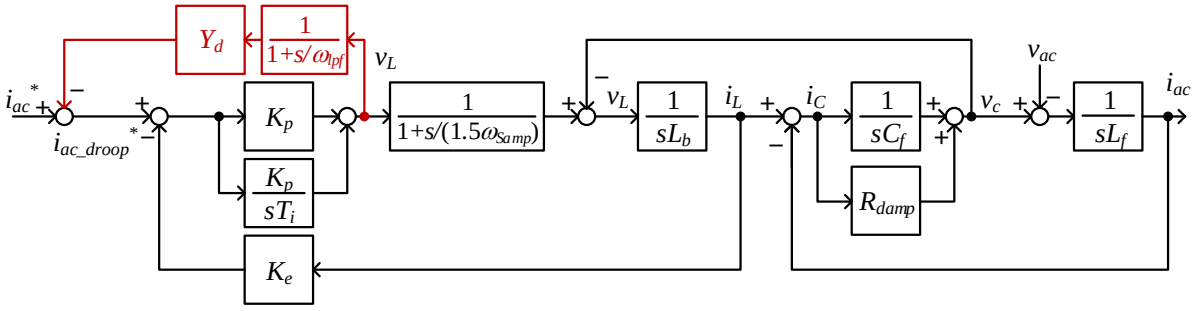


Figure 5. Control block diagram of USPM. The current droop control is implemented by the current droop gain Yd and LPF. In this paper, the change of the detection gain is considered.

The USPM controls the AC current without considering the DC voltage control for simplification of the controller. In the current droop control, a first-order LPF is inserted. The purpose of the LPF is not only to avoid recursive operations but also to avoid instability due to an increase in the droop gain. The current control of the module becomes unstable when LPF is replaced to one-sampling delay with very large current droop gain. The detailed reasons are shown in Figure 8. The current command value on the current droop control is given by;

$$i_{ac\_droop}{}^{*} = i_{ac}{}^{*} - Y_d \frac{1}{1+\frac{1}{2\pi f_{lpf}}s} v_L \quad (2),$$

where $i_{ac}{}^{*}$ is the current command value from the master controller, $i_{ac\_droop}{}^{*}$ is the current command value after applying the current droop control, v_L is the output of the current control, and f_{lpf} is the cutoff frequency of the LPF used for the current droop control.

The closed-loop transfer function $i_{ac\_x}(s)/i_{ac}{}^{*}(s)$ of the entire system and the AC output voltage characteristic $v_{ac\_x}(s)/i_{ac}{}^{*}(s)$ of each module are given by;

$$\frac{i_{ac}(s)}{i_{ac}{}^{*}(s)} = \sum_{x=1}^{k} \frac{i_{ac\_x}(s)}{v_{ac\_x}(s)} \left(\sum_{x=1}^{k} \left(\frac{v_{ac\_x}(s)}{i_{ac\_x}(s)} \frac{i_{ac\_x}(s)}{i_{ac}{}^{*}(s)} \right) - \frac{v_{ac}(s)}{i_{ac}{}^{*}(s)} \right) \quad (3)$$

$$\frac{v_{ac\_x}(s)}{i_{ac}{}^{*}(s)} = \frac{v_{ac\_x}(s)}{i_{ac\_x}(s)} \left(\frac{i_{ac\_x}(s)}{i_{ac}{}^{*}(s)} - \frac{i_{ac}(s)}{i_{ac}{}^{*}(s)} \right) \quad (4),$$

where i_{ac_x} and Y_{d_x} correspond to the closed-loop transfer function $i_{ac\_x}(s)/i_{ac}{}^{*}(s)$ and the disturbance rejection characteristics $v_{ac\_x}(s)/i_{ac}{}^{*}(s)$, respectively. The equation for designing the current droop gain is obtained from these characteristics.

IV. Design Method of Droop Control

Table 1 shows the parameters for the analysis of two series-connected control current source modules. In order to simulate the unbalance caused by the current sensing of the control current source modules, the sensing gain error E_{rr} is inserted only in module 1. $Y_{d\_p.u.}$ is set so that the rated admittance of the current source module is 1 p.u.

Figure 6 shows the bode plot of only the gain of the controller when Y_d is varied from 0p.u. to 1p.u. In Figure 6, the gain decreases as Y_d increases due to the limitation of the low bandwidth gain by the current droop control. The advantages of responsiveness and disturbance suppression characteristics cease to exist when the gain is reduced to the same level as that of P control. In addition, the gain reduced by the current droop control is already constant at around the operating frequency. Note that the current control bandwidth must be sufficiently higher than the operating frequency because the AC voltage phase of each USPM shifts due to the gain and phase characteristics not being constant when the current control bandwidth and current droop gain are low.

Figure 7 shows the characteristics of the open-loop transfer function with the current droop gain Y_d is varied from 0 p.u. to

Table 1. Parameters for the analysis of two series-connected control current source cells

USPM Parametar		
Rated Power	P	500 W
AC Rated Voltage	V_{acn}	100 V
AC Frequency	f_{ac}	50 Hz
DC link Voltage	V_{dc}	200 V
Filter Inductor	L_f	324 μH(%Z:0.51%)
Filter Capacitor	C_f	1.56μF(%Y:0.98%)
Boost Inductor	L_b	324 μH(%Z:0.51%)
Damping Resistor	R_{damp}	2 Ω
DC link Capacitor	C_{dc}	480 μF(H:19.2 ms)
Switching Frequency	f_{sw}	80 kHz
Sampling Frequency	f_{samp}	80 kHz
Dead-Time	T_d	200 ns
Controller Parameter		
Cutoff Freq. of Current	f_{c_acr}	5000 Hz
Cutoff Freq. of Voltage	f_{c_avr}	1 Hz
Voltage Det. Gain (Cell 1)	K_{e_1}	0.9
Voltage Det. Gain (Cell 2)	K_{e_2}	1.0
Maximum AC current deviation	δI_{max}	±30.0%

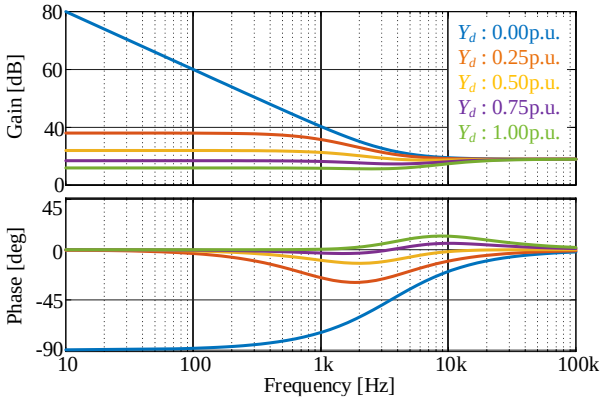


Figure 6. Bode plot of controller gain when Y_d is changed. The current droop control is designed with a decreasing and constant gain in the low band.

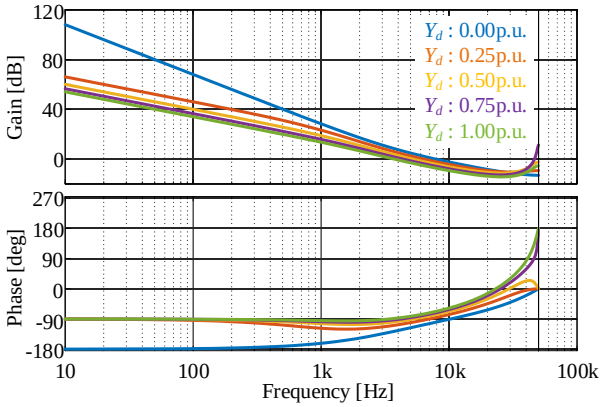


Figure 7. Characteristics of the open-loop transfer function. It is confirmed that the system is unstable at high droop gain around 50 kHz.

1 p.u. when LPF applied to the current droop control is replaced to one sampling delay. The current control becomes unstable due to the increase of the current droop gain. This instability is caused by the fact that the phase is delayed by 180 degrees without the gain falling even near the sampling frequency. Therefore, the delay should be LPF instead of the one sampling delay. The cutoff frequency of LPF is shown in detail in Figure 8.

Figure 8 shows the bode plot of the controller gain when the bandwidth of LPF inserted in the current droop control is varied from 50 Hz to 500 Hz. The gain characteristics are similar to those of the PR control because the poles and zeros become closer to each other as the cutoff frequency of the LPF applied to the current droop control approaches the operating frequency. In addition, the gain characteristic becomes like the phase-lead-lag compensation when the cutoff frequency of the LPF is high. The cutoff frequency of the LPF applied to the current droop control must be as high as possible. There are two reasons for that. One is that USPM requires constant gain over wide bandwidth.. The other is that overmodulation due to high gain needs to be avoided. Therefore, the cutoff frequency of LPF should be set equal to the cutoff frequency of the current controller in order to have wide bandwidth as possible.

Figure 9 shows the current deviation δI of the system when the current droop gain Y_d and the detection gain error E_{rr} are varied. Here, δI is the value obtained by subtracting the current command value from (3) and normalizing it by the current command value. The coating area indicates the area where the current deviation is not less than the desired value, the shaded area indicates the overmodulated area where the maximum AC voltage value V_{ac_max} obtained from (4) is higher than the minimum DC link voltage value V_{dc_min}. In Figure 9, δI is set to be less than ±30% and the ratio of V_{ac_max} to V_{dc_min} is set to be $2^{1/2}$. The overmodulation condition is unique to the current droop control in that there is no limit to the voltage droop control. The boundary condition of Y_d to satisfy the conditions of the current deviation and the overmodulation for each E_{rr} is obtained by solving the transfer function at 0 Hz using the fact that the gain characteristics below the operating frequency is constant. The current source and the parallel resistance on the equivalent circuit are given by;

$$\frac{i_{ac\_x}(s=0)}{i_{ac}^{*}(s=0)} = \frac{1}{K_{e\_x}} \tag{5}$$

$$\frac{i_{ac\_x}(s=0)}{v_{ac}(s=0)} = -\frac{Y_d}{K_{e\_x}} \tag{6}.$$

(5) and (6) are easily obtained by the detection gain and the current droop gain. Applying (5) and (6) to (3) and (4), the lower and upper limits of the current droop gain are given by

$$Y_d[p.u.] \le \left((1+\delta I)\frac{\sum_{y=1}^{k} K_{e\_y}}{k} - 1 \right) \frac{R_n}{R_{out}} \tag{7}$$

$$Y_d[p.u.] \ge \frac{\left(K_{e\_x} - \frac{\sum_{y=1}^{k} K_{e\_y}}{k} \right)}{\frac{V_{dc\_\min}}{V_{ac\_\max}} \frac{\sum_{y=1}^{k} K_{e\_y}}{k} - K_{e\_x}} \frac{R_n}{R_{out}} \tag{8};$$

where R_n is the rated impedance of the module, and R_{out} is the output impedance of the module. All controlled current source modules satisfy (7) and (8) to implement a highly responsive and steady current droop control without overmodulation. There are two main design guidelines for Y_d. One is the design to make the current response characteristic highly responsive (case1), and the other is the design to allow a wide range of detection error (case2). In case1, Y_d is set to be the critical condition in (8) given by;

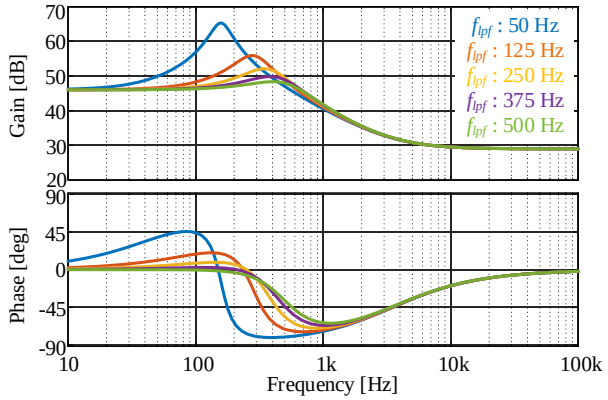


Figure 8. Bode plot of controller gain when f_{lpf} is changed. The design with high f_{lpf} avoids overmodulation due to high gain. The controller gain characteristics become more like the phase compensation at higher frequencies.

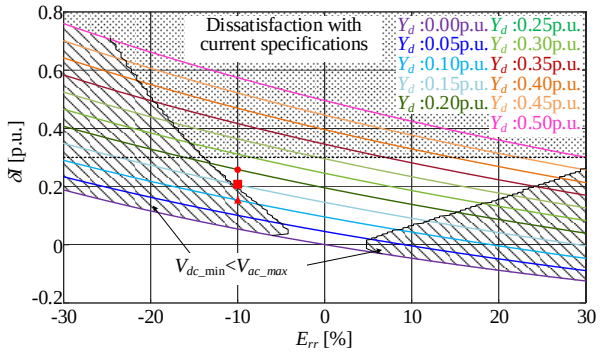


Figure 9. Characteristics of the current deviation in Y_d and E_{rr}. The design of Y_d should satisfy the current deviation condition and the overmodulation condition. The two points show design points that have been verified by experiments.

$$Y_d[p.u.] = \frac{\left(K_{e\_x} - \frac{\sum_{y=1}^{k} K_{e\_y}}{k}\right)}{\frac{V_{dc\_\min}}{V_{ac\_\max}} \frac{\sum_{y=1}^{k} K_{e\_y}}{k} - K_{e\_x}} \frac{R_n}{R_{out}} \quad (9).$$

In case 2, Y_d is set to be the matching condition of (7) and (8) given by;

$$Y_{d\_p.u.} = \left(\frac{\frac{V_{dc\_\min}}{V_{ac\_\max}} - 1 + (1 - E_{rr})(1 + \delta I)}{\frac{V_{dc\_\min}}{V_{ac\_\max}}} - 1 \right) \frac{R_n}{R_{out}} \quad (10).$$

In this paper, the design was done using $Y_{d\_p.u.}$ = 0.2 near case 2 in order to achieve the stable and wide acceptable detection error range. In the next chapter, the verification is done under the conditions of red circles and red squares in the overmodulated region designed in case 2 in Figure 9.

V. Simuration and Experimental Resurt

Figure 10 shows the droop characteristics in the current droop control when the current droop gain $Y_{d\_p.u.}$ is varied from 0.05 p.u. to 0.45 p.u. in regenerative operation. Note that only the current control and the current droop control are implemented in the USPM. In Figure 10, the system current increases with the increase of the droop gain and agrees with the characteristic by (1) with a maximum error of 3.5%. The main reason for the error is that there was originally a detection gain error in the detection circuit.

Figure 11 shows the simulation results under the conditions of red circle ($Y_{d\_p.u.}$ = 0.2p.u.), red square ($Y_{d\_p.u.}$ = 0.15p.u.) and red triangle ($Y_{d\_p.u.}$ = 0.1p.u.) in Figure 9. In Figure 11, the current command value i_{ac} is a sinusoidal wave synchronized with the phase of the grid voltage v_{ac}. Under the condition of $Y_{d\_p.u.}$ = 0.1p.u., the AC current has a overmodulation near the peak because the amplitude of the AC voltage is larger than the DC link voltage. This overmodulation is caused by the unbalance of the output of each USPM due to the detection gain error. In addition, the reactive power is generated at the power factor of 0.996 and 0.968 for each USPM. This reduction in power factor is caused by the phase delay near the operating frequency. Therefore, it is necessary to reduce the phase delay by PLL processing in each USPM or by using a high current control bandwidth. Here, the current THD is 0.97%. Under the condition of $Y_{d\_p.u.}$ = 0.15p.u., the AC current THD is 0.43% because the AC voltage avoids overmodulation near the DC link voltage. The current deviation under this condition is 20.2%, which corresponds to a current error of 1.05% from the calculated equation. This result shows the high accuracy of the derived equation: the condition of $Y_{d\_p.u.}$ = 0.2p.u. results in a low THD of 0.48% AC current THD, similar to the condition of $Y_{d\_p.u.}$ = 0.15p.u.

Figure 12 shows the experimental results. Note that the current command amplitude is set to 60% of the rated current, hence the current droop gain is also set to 60% of the design point in Figure 9. Thus, $Y_{d\_p.u.}$ at the red circle is 0.12p.u., $Y_{d\_p.u.}$ at the red square is 0.09p.u., and $Y_{d\_p.u.}$ at the red triangle is 0.06p.u. The phase of the current command is synchronized with the phase of the AC voltage v_{ac_x} at each USPM. Under the condition of $Y_{d\_p.u.}$ = 0.06p.u., the voltage THD at each USPM is 13.3% and 5.16% due to the overmodulation caused by the current detection gain error. The phase is hardly out of phase because it is corrected by the PLL process in each USPM. Furthermore, this difference becomes smaller when the bandwidth of the current control is extended. However, the risk of instability due to phase lock release increases when the voltage THD increases any further. Here, the THD of the

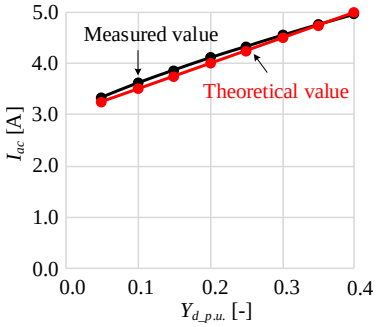
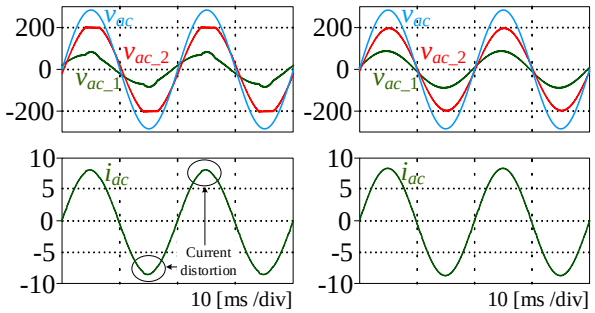
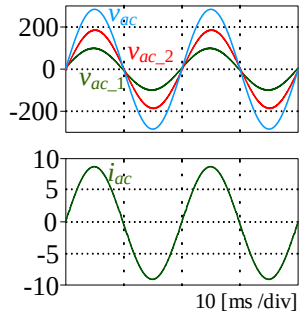


Figure 10. Droop characteristics of the current droop control. Measured values match well with theoretical values.



(a) $Y_{d\_p.u.}$: 0.1p.u. (b) $Y_{d\_p.u.}$: 0.15p.u.



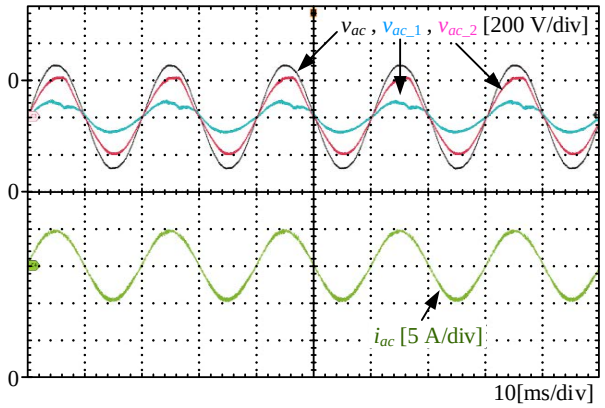
(c) $Y_{d\_p.u.}$: 0.2p.u.

Figure 11. Simulation results when droop gain is changed. The input current is decoupled by Y_d. The current distortion occurs due to the overmodulation.

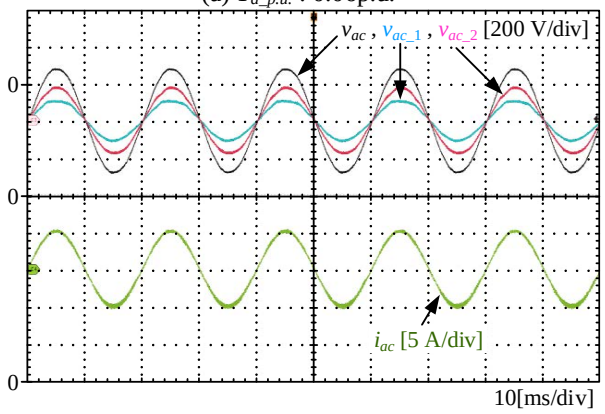
current is 1.67%. The current deviation is 12.2% which corresponds to the current error of 3.15% from the formula. The main reason for the error is that there was originally a detection gain error in the detection circuit. Under the condition of $Y_{d\_p.u.}$ = 0.12p.u., the AC voltage unbalance is suppressed and no overmodulation occurs. Here, the THD of the AC current is improved to1.26%. The current deviation is increased to 22.4% due to the increase in the current droop gain. The current error from the formula corresponds to 3.17%. The main reason for the current error in Figure 12 is the error caused by the original current detection as in Figure 11.

VI. Concrusion

In this paper, the concept of the universal smart power module including the high-speed controller and some additional functional blocks was proposed for the further user-friendly design and scalability of the modular power conversion systems. Furthermore, the current droop control and its design method are proposed as a decoupling technique required for the series-connected USPMs. The proposed method is considered in the duality with the voltage droop control. The current droop gain is easily implemented from the mathematical equations. The experimental result with the series-connected USPMs demonstrate that the proposed method eliminates the current distortion caused by overmodulation. In addition, the current deviation in the experiment was coincident with the current deviation in the design with an error of 3.17%.



(a) $Y_{d\_p.u.}$: 0.06p.u.



(b) $Y_{d\_p.u.}$: 0.12p.u.

Figure 12. Experimental results when droop gain is changed. The overmodulation due to the detection gain error is avoided by increasing Y_d.

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