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Paper

Isolated DC to Single-Phase AC Converter with Active Power Decoupling Capability Using Coupled Inductor

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This paper proposes a novel active power decoupling circuit that is integrated with an interleaved boost converter for isolated DC to single-phase AC conversion applications. The proposed isolated converter consists of two full-bridge inverters with a coupled inductor, a small buffer capacitor for active power decoupling, and a diode rectifier. Further, the proposed isolated converter is controlled for active power decoupling and DC to single-phase AC power conversion independently by the coupling inductor and common-mode operation of the interleaved boost converter, respectively. This paper presents the control method of the proposed converter and design criteria of the passive components. In addition, the performance of the proposed isolated converter is demonstrated by the experimental results in order to confirm the validity of the proposed method. As the experimental results, the second-order harmonic due to the double-line frequency power ripple is reduced by 84.5% owing to the active power decoupling capability. Finally, a maximum efficiency of 94.5% is obtained using the proposed converter.

Keywords : Isolated DC to single-phase AC converter, Power decoupling, Coupled inductor;

1. Introduction

Recently, a Fuel Cell (FC) has been widely accepted as the renewable energy sources for the energy saving [1-2]. The power conditioning systems (PCSs) are the one of the applications for FC, and it may become a trend for next power generation systems as same as photovoltaic systems. PCSs require some capabilities: (1) boost-up function of the FC voltage, (2) galvanic isolation, and (3) power decoupling capability between DC and single-phase AC. In order to satisfy these requirements, PCSs typically consist of an isolated DC to single-phase AC converter which includes the boost converter, isolated DC/DC converter, and a voltage source inverter.

In addition, a lot of circuit configurations for PCSs have been studied in order to achieve the high-power density. The interleaved boost converter is one of good options for the reduction of the volume of the boost inductor because the current ripple is cancelled by the phase-shifted operation regardless of the small inductor [3-6]. In addition, the coupled inductor shares the multi winding during each phase, and the number of cores is reduced in comparison with the multi-phase interleaved converter.

On the other hand, the double-line frequency power ripple is the one of the primitive issues for the single-phase application because it fluctuates the DC power with the twice of the grid frequency. Therefore, a bulky electrolytic capacitor is generally placed on the DC-link to absorb the power ripple. It is do called “passive power decoupling”. However, the electrolytic capacitors may limit the life-time, and increases the circuit volume [7].

In contrast, active power decoupling, which uses passive components with active switches, circuits have been proposed in order to solve this problem [8-15]. In these methods, the double-line frequency power ripple is compensated by the small capacitor which permit the large voltage fluctuation. As a result, the small capacitor such as firm or ceramic capacitor is chosen for the DC-link capacitor and the active power decoupling capacitor. However, almost conventional active power decoupling circuits require the additional components including the passive components and the switching devices for the active power decoupling circuit and also decrease the power density of the isolated converter. Therefore, the active power decoupling method with few additional components is required in order to achieve the high-power density converter [14].

This paper proposes a novel isolated DC to single-phase AC converter with active power decoupling capability. This coupled inductor is integrated into the boost chopper of the interleaved converter and the active power decoupling circuit by setting the third winding to the coupled inductor. This integrated circuit using the coupled inductor is achieved to control the common-voltage as an active power decoupling operation mode and the differential-voltage as an operation mode of a power conversion with the galvanic isolation independently. Therefore, the proposed converter greatly reduces the number of the switching devices and additional components for the active power decoupling circuit. In addition, the secondary side of the proposed converter reduces the switching losses because the secondary side converter is operated at the twice grid frequency to only control the polarity conversion. Thus, the proposed converter can be expected to achieve the high-power density and the long-lifetime. It is noted that the integrated topology into the active power decoupling capability and the power conversion have been researched in the past work [16-19]. These active power decoupling methods do not require additional switching devices by applying common and differential operation modes to the interleave topology. However, these active power decoupling methods have problems that there are plural additional

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energy components for the active power decoupling circuit. In the solution method of the elimination of the additional components for the active power decoupling circuit, the isolated converter with the center-tapped transformer has been reported in [18]. This active power decoupling topology is eliminated the additional switching devices and consists only one buffer capacitor and one buffer inductor, but that the required capacity of the energy buffer components increases in the case of the low input DC voltage.

The originality of this active power decoupling topology is not required for any additional components, owing to the employment of the coupled inductor. In addition, the proposed method verifies the active power decoupling capability in the low input DC voltage. This active power decoupling method by using the coupled inductor was also introduced in [21]. However, in this paper, only the basic verification of the scale model is reported, and the detailed designing method of the circuit condition and the coupled inductor to realize the proposed control method and the active power decoupling capability is not clarified. Thus, the circuit presented in [21] is not reproducible and unclear whether it can achieve a high-efficiency.

This paper focuses on clarifying the designing flow and the verifying superiority of the proposed method based on the analysis results of the conventional circuit in [21]. Furthermore, it was confirmed by the experimental analysis that the semiconductor losses are reduced compared to the conventional circuit with the active power decoupling capability.

This paper is organized as follows; first, the proposed converter for the DC to single-phase AC converter and the principle of the active power decoupling method are introduced; second, the operation mode of the proposed converter and the modulation methods with the active power decoupling capability and the designing flow of the coupled inductor are explained; finally, the fundamental operation waveforms of the proposed converter are evaluated in experiments.

2. Circuit Topology

2.1 Conventional Circuit

Figure 1 shows a conventional isolated DC to single-phase AC converter. This converter consists of an interleaved boost converter, an isolated DC to DC converter, and a full bridge inverter. The interleaved boost converter has the capability of the boost-up of the input voltage. This two-phase interleaved topology is employed to reduce the conduction loss and the volume of the boost inductor. In addition, the full bridge inverter at the primary side generates a high-frequency square voltage to reduce the volume of the transformer. However, a bulky electrolytic capacitor C_{dc2} is typically required on the DC-link in order to compensate the double-line frequency power ripple.

Figure 2 shows the isolated DC to single-phase AC converter with the conventional active power decoupling circuit. The conventional active power decoupling circuit in Fig. 2 consists of two additional switching devices and two passive components. The conventional active power decoupling circuit regulates the buffer capacitor voltage, and the power ripple is absorbed by the small capacitor of C_{buf}. However, these additional components increase the circuit volume and decrease the conversion efficiency. In particular, the addition of the magnetic component constricts the high-power density of the converter system.

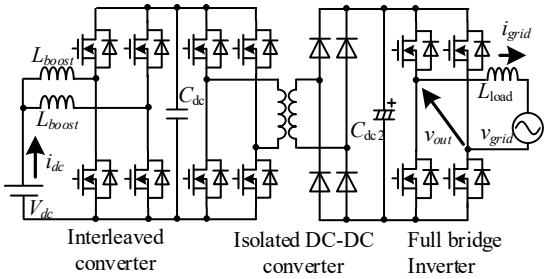


Fig. 1. Conventional isolated DC to single-phase AC converter with interleaved boost topology. The conventional converter uses a bulky electrolytic capacitor C_{dc} to absorb the power ripple component caused by a single-phase ac load.

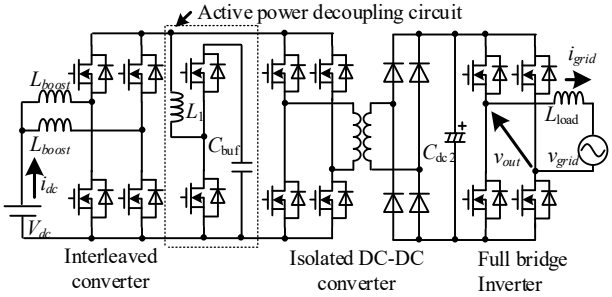


Fig. 2. Conventional isolated DC to single-phase AC converter with active power decoupling circuit. The conventional active power decoupling circuit consists of few passive components and switching devices.

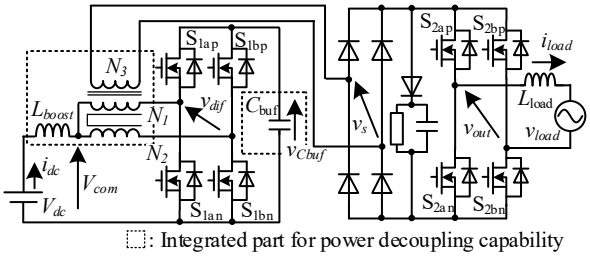


Fig. 3. Proposed isolated DC to single-phase AC converter. The primary-side converter together with the coupled inductor and the buffer capacitor are controlled in order to convert the DC input power to the AC output power and absorb the power ripple without additional switching devices and inductors.

2.2 Proposed Circuit

Figure 3 shows the proposed isolated DC to single-phase AC converter with the active power decoupling capability. The proposed converter consists of two full bridge inverters, the buffer capacitor, the diode rectifier and the coupled inductor. The proposed converter integrates with the active power decoupling circuit, interleaved boost converter, and isolated DC/DC converter in order to reduce the number of components. The proposed method is operated two operations as an active power decoupling and a power conversion at the same time by applying the common and differential voltage control with the coupled inductor. The active power decoupling control is employed with a common mode operation, whereas the grid current control is implemented with a differential mode operation.

The secondary converter converts the high-frequency AC to the single-phase line frequency AC without DC-link. The secondary converter performs the rectifier operation and the polarity reversion

of the input voltage to output the grid voltage. Therefore, the switching loss of the secondary full-bridge inverter is smaller by applying the polarity reversion at 50 Hz. The snubber circuit, which connected between the diode rectifier and the full-bridge inverter, has a role of an absorbing surge generated by the connection between the load inductor, the leakage inductor and the boost inductor. Note that the resistor in the RCD snubber circuit is to discharge the stored energy in the snubber capacitor. The proposed converter realizes the DC to single-phase AC power conversion and the active power decoupling capability with lower the number of the components in comparison with the configuration of Fig. 2.

3. Control Strategy

3.1 Parameter design of Active Power Decoupling

Figure 4 shows the principle of the active power decoupling method. It is assumed that firstly, the instantaneous single-phase AC power p_{out} is expressed as

$$\begin{aligned} p_{out} &= \sqrt{2}V_{load}\sin(\omega_o t)\cdot\sqrt{2}I_{load}\sin(\omega_o t) \\ &= V_{load}I_{load}\{1-\cos(2\omega_o t)\} \\ &= P_{ave}-P_{ave}\cos(2\omega_o t) \end{aligned} \quad \text{..... (1),}$$

where V_{load} and I_{load} is the root-mean-square (rms) value of the output voltage and current, ω_o is the grid side angular frequency and P_{ave} is the average output power. Note that a grid current i_{grid} and voltage v_{grid} are a sinusoidal waveform with a unity power factor. In order to obtain a constant value of the input current at the DC side, the ripple component should be eliminated. Thus, the buffer power p_{buf}, which absorbs the power ripple component generated by a single-phase AC load is assumed by the following:

$$p_{buf} = P_{ave}\cos(2\omega_o t) \quad \text{..... (2).}$$

The polarity of the buffer power is defined to be positive when the buffer capacitor is charged.

$$\begin{aligned} P_C &= \frac{1}{2}\omega_o C_{buf} {v_{Cbuf}}^2 \\ &= \frac{1}{2}\omega_o C_{buf}\left\{\left(v_{ave}+\frac{\Delta v_c}{2}\right)^2-\left(v_{ave}-\frac{\Delta v_c}{2}\right)^2\right\} \end{aligned} \quad \text{..... (3),}$$

where v_{ave} is the average voltage of the buffer capacitor and Δv_c is the peak-to-peak of the buffer capacitor voltage range. The buffer capacitor voltage v_{Cbuf} which needs to absorb the power ripple is calculated based on the energy of the buffer capacitor. First, the energy of the buffer capacitor W_{Cbuf} is expressed by a voltage-current equation of a capacitor and (2).

$$\begin{aligned} W_{Cbuf} &= \int_{t_0}^{t} v_{Cbuf}\left(C_{buf}\frac{dv_{Cbuf}}{dt}\right)dt \\ &= \int_{t_0}^{t} P_{ave}\cos(2\omega_o\tau)\,dt \end{aligned} \quad \text{..... (4)}$$

By using (4), the buffer capacitor voltage to compensate the power ripple is presented by the following:

$$v_{Cbuf} = \sqrt{{V_{C0}}^2+\frac{P_{ave}}{\omega_o C_{buf}}\sin(2\omega_o t)} \quad \text{..... (5),}$$

where V_{co} is the buffer capacitor voltage at a start time t_0. In the proposed converter, the input current i_{dc} flowing to the coupled inductor from DC supply is controlled as a constant DC value. Thus, the buffer capacitor voltage has the power ripple components. The proposed converter with the active power decoupling capability is achieved, whose result is that the power ripple component at DC side is absorbed.

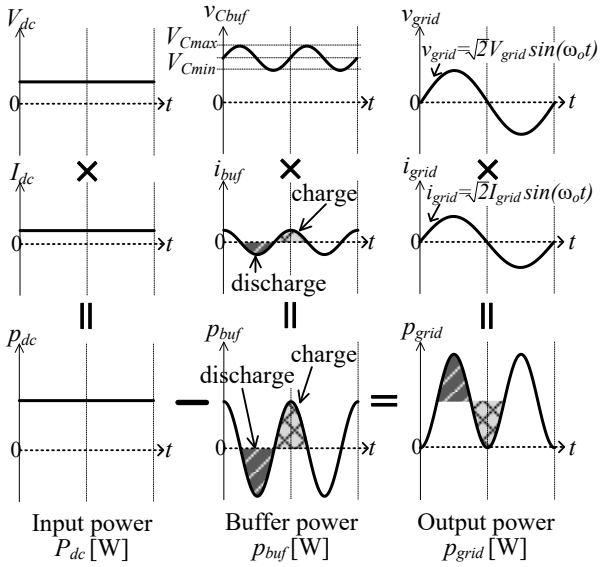


Fig. 4. Relationship among each waveform.

The buffer capacitor in the active power decoupling is calculated by

$$C_{buf} = \frac{P_{ave}}{\omega_o v_{ave}\Delta v_c} \quad \text{..... (6).}$$

In the case with the active power decoupling method, the buffer capacitor voltage is controlled to large Δv_c. Then, the required storage energy is achieved with small capacitance. This is the principle to be able to reduce the capacitance in the active power decoupling circuits. It should be noted that the limited bottom value of the buffer capacitance is decided by the voltage capacity of the switching devices in the primary-side. In addition, the average voltage v_{ave} inevitably becomes the twice of the input voltage V_{dc}, which the turn number N_1 is equal to the turn number N_2 of the coupled inductor. The designing method of the turn numbers of the coupled inductor is explained in the fourth section.

3.2 Duty Calculation

Figure 5 shows the operation modes of the primary-side converter. The proposed primary-side converter has four operation modes which generate a phase difference between the switching timing of each arm as an interleaved converter. The boost inductor L_{boost} is a leakage inductor of the transformer, and it is utilized for the boost operation and the current control for the active power decoupling operation. Note that if the inductance value of the leakage inductor is insufficient for the designing value, a small inductor may be added. The boost inductor is decided by the current ripple ratio in the worst case, which is calculated by using the maximum on-duty ratio of the common mode operation.

$$L_{boost} = \frac{d_{com\_mux}V_{dc}}{2\Delta i_{dc}f_{sw}} \quad \text{..... (7),}$$

$$\Delta i_{dc} = \frac{i_{ripple\_pp}/2}{i_{dc}} \quad \text{..... (8)}$$

where Δi_{dc} is the allowable current ripple ratio, i_{ripple_pp} is the peak to peak value of the input current and f_{sw} is the switching frequency

of the interleaved converter. Note that the d_{com_max} is the maximum reference of the common mode operation in one period, which is explained in detail in the next section.

In the proposed system, the differential-mode voltage of the coupled inductor is controlled to generate the output current, whereas the common-mode voltage is controlled to perform the active power decoupling capability. In the control of the differential-mode voltage, the three-winding voltage of the coupled inductor is controlled into a three-level voltage by operation modes as shown in Fig. 5 (a) and (b).

On the other hand, the common-mode voltage v_{com} is controlled to absorb the power ripple in the control of the common mode voltage. Especially, the power ripple component occurs in the buffer capacitor voltage, because the input current is regulated into a constant value in the active power decoupling method of the proposed converter. Moreover, the active power decoupling capability consists of a boost topology in the proposed operation. The coupled inductor is boosted the fluctuation of the buffer capacitor voltage in bigger than the input voltage V_{dc}. The capacitance of the buffer capacitor is achieved to reduce enough to increase the fluctuated voltage of the buffer capacitor to absorb the power ripple component. Thus, the proposed converter with the boost topology of the active power decoupling capability is achieved to reduce the capacitance than a buck-type topology of the one [14].

Each duties of the primary converter in one carrier period should satisfy the following requirement:

$$1 = d_{dif\_a} + d_{dif\_b} + d_{com\_c} + d_{com\_d} \quad \text{..... (9)}$$

where d_{dif_a} and d_{dif_b} are the duties of the differential mode operation as shown in Fig. 5 (a) and (b), whereas d_{com_c} and d_{com_d} are the duties of the common mode operation as shown in Fig. 5(c) and (d). If the output voltage for the grid side is controlled into a sinusoidal waveform, the voltage pulses between the first and second winding are controlled as PWM pulses. The sum duties d_{dif} of the differential mode operation is given by

$$\begin{aligned} d_{dif} &= d_{dif\_a} + d_{dif\_b} \\ &= \left| \frac{v_{out}^{*}}{v_{Cbuf}} \right| = \left| \frac{\sqrt{2} V_{load} \sin(\omega_o t)}{v_{Cbuf}} \right| \end{aligned} \quad \text{..... (10)}$$

where v_{out}^{*} is a command of the output voltage as a grid-side.

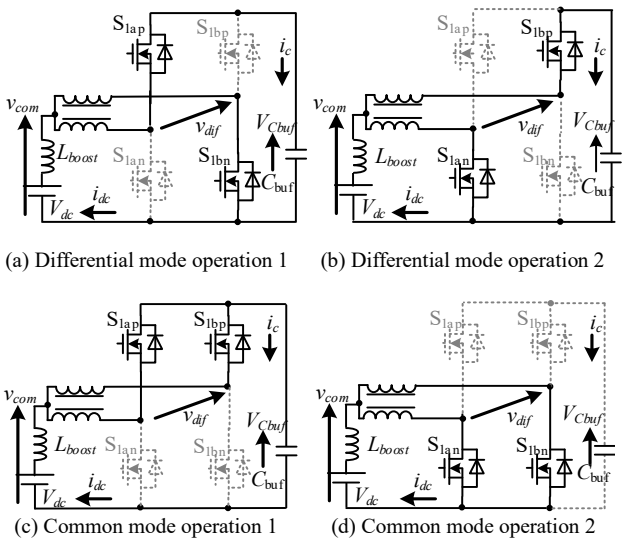
In contrast, the duty of the common mode operation is expressed by using the calculation result from (10) in order to meet the control condition (9).

$$d_{com} = d_{com\_c} = (1 - d_{dif}) \frac{v_{com}^{*}}{v_{Cbuf}} \quad \text{.....(11)}$$

where v_{com}^{*} is a voltage command of the common mode operation, which is output command by the input current control as explained in the next section. The maximum on duty ratio of the common mode operation is around the zero-voltage period of the grid voltage as shown in (11). The maximum on duty of the common mode operation d_{com_max}, which has the condition of the worst case of the current ripple ratio is presented by

$$d_{com\_\max} = \frac{v_{com}^{*}}{V_{C0}} = \frac{v_{com}^{*}}{2V_{dc}} \quad \text{..... (12).}$$

In the case of the zero-voltage period of the grid voltage, the buffer capacitor voltage becomes the average voltage as a twice of DC input voltage by using same turn numbers between the first and second winding of the coupled inductor. Thus, the on duties of the common mode operations as shown in Fig. 5(c) and (d) are equalized to keep the average voltage of the buffer capacitor, so maximum on duty of the common mode operation in one switching period is divided equally to 0.5.



(a) Differential mode operation 1 (b) Differential mode operation 2

(c) Common mode operation 1 (d) Common mode operation 2

Fig. 5. Operation modes of primary-side converter with coupled inductor.

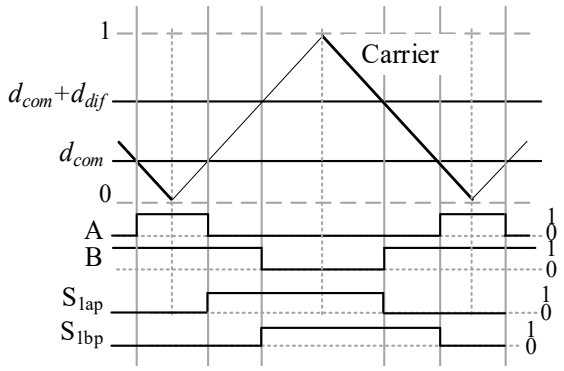


Fig. 6. Relationship between gate signal and each command in primary converter.

Figure 6 shows the relationship among each command, the triangle carrier and the gate signals of the primary converter. In the differential mode operation, the differential voltage pulses between the first and second winding are controlled as PWM pulses. Then, the period of each duty as shown in Fig. 5 (a) and (b) in one carrier period is needed to be equal in order to suppress a DC biased magnetization of the transformer, especially. The comparing signals A and B are generated by comprised duties which the sum of d_{com} and d_{dif}, only d_{com} and a triangle carrier as shown in Fig. 6. Therefore, the desired operation in each duty of the primary converter is actualized as described previously.

Figure 7 shows the control block diagram of the proposed converter with the active power decoupling capability. The current controls and the voltage control are employed with PI controllers. The input current is controlled to a constant DC value to absorb the double-frequency power ripple component. This input current control is applying as a minor loop of the buffer capacitor voltage control. This buffer capacitor control controls only the average of

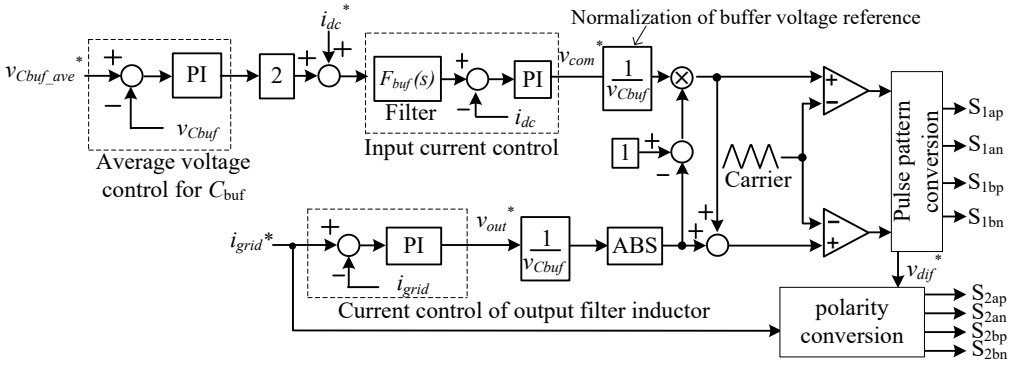


Fig. 7. Proposed control block diagram. The DC current is controlled to absorb power ripple. The buffer capacitor voltage control is employed in order to avoid the divergence of the average voltage due to discretization.

the buffer capacitor voltage v_{Cbuf_ave} in order to avoid the divergence. The average value of the buffer capacitor voltage v_{Cbuf_ave} is twice of the input voltage V_{dc}. In the proposed converter, the output current is controlled by the full bridge inverter at the primary side. Then, the secondary converter has the role as the rectifier and the polarity conversion.

4. Designing Method of Coupled Inductor

The coupled inductor of the proposed converter used for a galvanic isolation at the power conversion and the current control for the active power decoupling operation and the power conversion to single-phase AC side. The designing method and each turn number of the coupled inductor in the proposed converter is explained in this section.

Figure 8 shows the flowchart of the designing method for the coupled inductor in the proposed converter. The designing condition as input elements for the starting flowchart is that f_{sw} is the switching frequency of the interleaved converter, K_u is a window utilization factor and J is a current density of a winding. The voltage and current values of other input elements are setup to refer an application of the converter system. It is noted that the coupled inductor of the proposed converter definitely is made by using only one core in order to cancel each magnetic effect.

First, these parameters of the core are decided by used to refer the switching frequency, which is selected by the semiconductor devices and the rated power of the converter system. In the proposed converter, the switching frequency of the interleaved converter is decided on 50 kHz by applying the SiC semiconductor devices in this paper. The parameters as output elements of the selecting core are that A_e is a cross-sectional area, W is a winding area and B_s is a saturated magnetic flux of the core. These parameters have an influence on the selected core size.

Second, the coupled inductor with the third winding is designed by focus on the maximum magnetic flux density. In general, the magnetic flux density B_{ac} is expressed by using the area product method in [20],

$$B_{ac} = \frac{I_p V_p + I_3 V_3}{W A_e f_{sw} J K_u K_f} \quad \text{..... (13)}$$

where I_p is an input current as a sum of the first and second winding current, V_p is an input voltage as a sum of the first and second winding voltage, I_3 is a third winding current and V_3 is a third winding voltage. In addition, K_f is a waveform coefficient, which is decided by the kind of input waveform with square or sine wave for

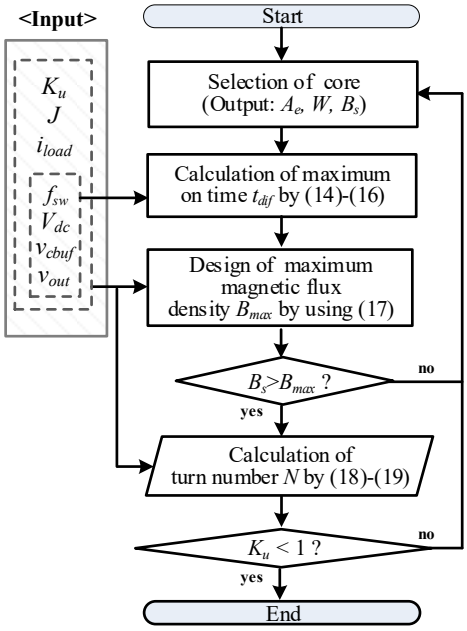
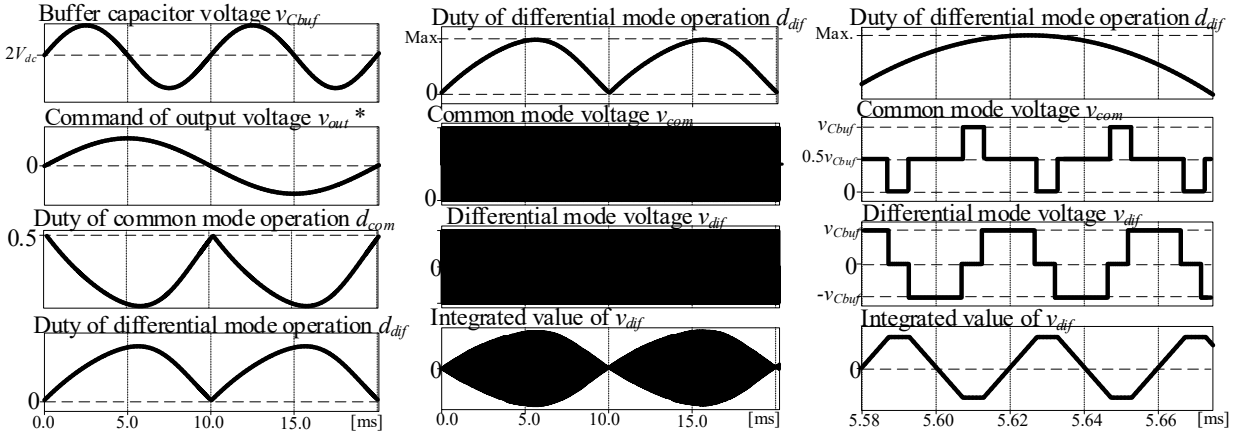


Fig. 8. Flowchart of designing method for coupled inductor.

a coupled inductor [20]. From (13), the maximum magnetic flux density is calculated by using a constant input voltage and a constant on-time in the switching period in general.

In the proposed operation, the input and the third winding voltage as a differential voltage v_{dif} are not a constant value but expressed by the PWM pulses with the twice of the grid frequency. Thus, the maximum magnetic flux density in the proposed operation depends on the twice of the grid frequency. The coupled inductor of the proposed converter requires the deriving condition; (1) differential voltage at the maximum point of the magnetic density, (2) maximum on-time of the differential mode operation.

Figure 9 shows each voltage command and the integrated waveform of the differential voltage in the proposed operation. The duties of the two operation modes as shown in Fig.9 (a) are distorted because they are calculated by using the square root of the twice of the grid frequency and the grid frequency in order to control with a normalization. On the other hand, Fig.9 (b) shows the voltage waveforms of the common and the differential mode operation, and Fig.9 (c) shows the expansion in Fig.9 (b). The differential-mode voltage is a three-level voltage waveform, which is combined of v_{Cbuf}, $-v_{Cbuf}$, and a zero-voltage period. The period of the zero-



(a) Each command waveform (b) Integrated value of differential voltage (c)Expansion of each waveform

Fig. 9. Relationship of differential voltage as input voltage for coupled inductor and integrated value of differential voltage. The integrated value of the differential mode voltage is fluctuated with the grid frequency because the gate signals of the differential mode is generated by PWM pulses as a grid sine waveform.

voltage level in the differential-mode voltage is utilized with the top and the bottom level of the common-mode voltage. From Fig.9 (b), the integrated value of the differential-mode voltage as a magnetic flux has an envelope curve caused by PWM operation and the twice of the grid frequency. Therefore, the magnetic flux density, which is proportional to the magnetic flux has the same envelope curve and the maximum value at the same phase as the maximum point of the duty d_{dif} in the proposed operation.

In order to derive the maximum magnetic flux density B_{max} in the proposed operation, it is needed to define the on-time of the differential mode operation, which is calculated by using the switching frequency and the duty of the differential mode operation d_{dif}. This on-time of the differential mode operation is used to replace from the waveform coefficient in (13) to the calculation condition of the proposed operation. The on-time of the differential mode operation t_{dif} is expressed by

$$t_{dif} = \frac{d_{dif}}{f_{sw}} = \frac{\sqrt{2}V_{load}\sin(\omega_o t)}{\sqrt{{V_{C0}}^2 + \frac{P_{ave}}{\omega_o C_{buf}}\sin(2\omega_o t)} \times f_{sw}} \quad \text{..... (14).}$$

The angular frequency $\omega_o{}'$ at the maximum on-time of the differential operation mode is given by

$$\arg\max t_{dif}(\omega_o t) \approx \frac{16}{25}\pi t = \omega_o{}' t \quad \text{..... (15).}$$

As described above, in the proposed operation, PWM operation for the grid current control is performed by using the normalization with the twice of the grid frequency. The maximum magnetic flux density deviates from the angular frequency at the maximum point of the on-time. The maximum on-time $t_{dif}(\omega_o{}')$ of the differential mode operation is represented by using (14)-(15) and (5),

$$t_{dif}(\omega_o{}') \approx \frac{0.91\sqrt{2}V_{load}}{\sqrt{{V_{C0}}^2 - 0.77\frac{P_{ave}}{\omega_o C_{buf}}} \times f_{sw}} \quad \text{..... (16).}$$

The maximum magnetic flux density in the proposed operation is represented as following;

$$B_{\max} = \frac{2i_{load}(\omega_o{}')v_{Cbuf}(\omega_o{}')t_{dif}(\omega_o{}')}{WA_e JK_u} \approx \frac{3.27I_{load}V_{load}}{WA_e JK_u f_{sw}} \quad \text{.....(17).}$$

Note that maximum magnetic flux density is calculated with the conditions, which are the same turn numbers between the input-side and third-winding side, and excluding the core loss. If the obtained result of the maximum magnetic flux density is smaller than the saturation magnetic flux density of the selected core, the designing condition is satisfied.

Finally, each turn number is calculated by using each voltage condition and the maximum magnetic flux density. The important point of the design for the coupled inductor is the turn ratio of the input-side, which consists the number of turns at the first-winding N_1 and the second-winding N_2 as shown in Fig. 3. The turn ratio N_1 vs N_2 makes sure to set up 1:1, because the effect of the magnetic flux at each winding are canceled each other by the same number of turns. Thus, the designing method is as same as a general transformer designing method regardless of the ripple component as a 50 Hz. The turn number is presented by

$$N = 0.5N_1 = 0.5N_2 = N_3 \quad \text{.....(18),}$$

$$N = \frac{v_{Cbuf}(\omega_o{}')t_{dif}(\omega_o{}')}{2B_{\max}A_e} \approx \frac{0.45\sqrt{2}V_{load}}{B_{\max}A_e f_{sw}} \quad \text{.....(19)}$$

where N_3 is the third-winding of the coupled inductor. For simplicity and voltage conditions, the turn ratio N_1+N_2 vs N_3 sets up 1:1 in this paper. The turn ratio is freely decided by the relationship with the input and the output voltage.

It is necessary to confirm whether the window utilization factor K_u exceeds 1.0 from the derived turn number and the winding area of the selected core W. If the window utilization factor is less than 1.0, the design of the coupled inductor with the three winding ends.

5. Experimental Results

Table 1 shows the experimental conditions with R-L load, and Figure 10 demonstrates the experimental waveforms of the proposed converter. It is noted that the unit capacitance constant in Table 1 is defined as the electrostatic energy of the capacitor divided

Table 1 Experimental condition

Input voltage	200 V_{dc}	Load voltage	200 V_{rms}
Rated power	2 kW	Load frequency	50 Hz
Boost Inductor (L_{boost})	1.1 mH	Filter Inductor (L_{out})	2.0 mH(3.1%)
Buffer Capacitor (C_{buf})	200 μF(8 ms)	Turn ratio of coupled inductor N_1:N_2:N_3	1 : 1 : 2
Load current	10 A_{rms}		
Carrier frequency of full bridge inverter	50 kHz	Switching frequency of secondary-inverter	50 Hz

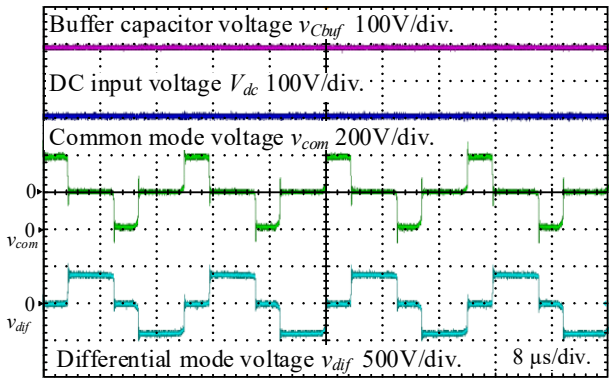
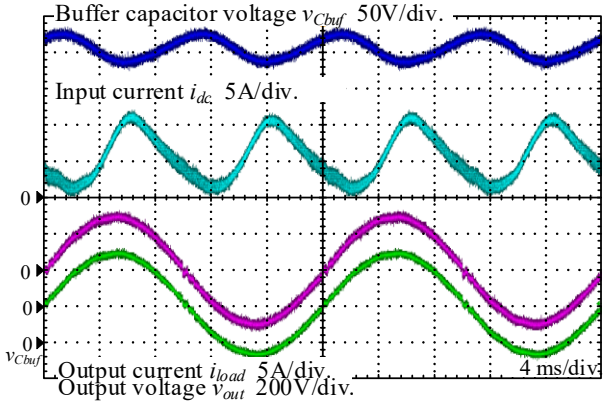


Fig. 10. Extension of each voltage waveforms. The maximum voltages of the two operation modes are decided by the buffer capacitor voltage with the twice grid frequency.

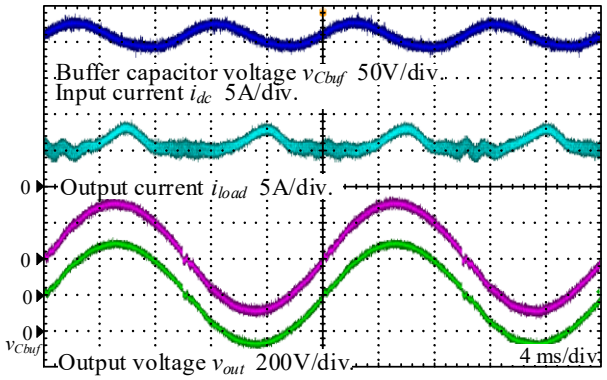
by the rated power of the converter, and its unit is "second" [22]. From the experimental waveforms with the coupled inductor, the fundamental operation of the proposed method was confirmed that the differential-mode voltage v_{dif} is a three-level voltage waveform based on a zero voltage. On the other hand, the common-mode voltage v_{com} is a three-level voltage based on a half of the buffer capacitor voltage. Therefore, the proposed converter greatly reduces the number of the switching devices and additional components for the active power decoupling circuit, owing to the employment of the coupled inductor.

Figure 11 shows the experimental results with and without the proposed active power decoupling method. In the experimental result without the active power decoupling operation as shown in Fig. 11 (a), the capacitance of the buffer capacitor C_{buf} is not enough to absorb the double-line frequency component on the dc side compared by using the electrolytic capacitors. As a result, the remaining double-line frequency component occurs to the dc input current. On the other hand, from Fig. 11 (b), the buffer capacitor voltage is operated to absorb the power ripple component. Therefore, the double-line frequency component on the dc input current was reduced to 14.6% at 1 kW. It is noted that the remaining double-line frequency component on the dc input current around the area of the maximum or minimum output voltage is caused that the duty of the common mode operation is limited in Fig. 11 (b).

Figure 12 shows the fundamental waveforms with the active power decoupling method in the lowest input voltage condition at 160 V_{dc}, which is worst case of the fluctuating input voltage. This experiment with the low input voltage is operational checks because it is necessary to take into account the DC input voltage may vary depending on the connected application. Note that the average voltage of the buffer capacitor is twice the input voltage, and the other condition in the low input voltage condition at 160 V_{dc} is the same to the setup as shown in Table 1. From the experimental results under the steady state, the good active power decoupling capability is confirmed by the proposed method.



(a) Without active power decoupling method



(b) With active power decoupling method.

Fig. 11. Experimental waveforms in steady state when output power is about 1 kW. The buffer capacitor voltage is absorbing the double-line frequency power ripple component on the input current.

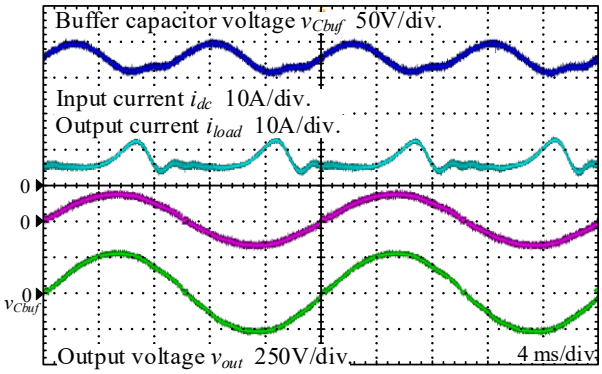


Fig. 12 Waveforms of proposed isolated converter with active power decoupling method and low input voltage condition at 1 kW. This experimental result is limited to compensated capability at the point between the bottom of the buffer capacitor voltage and the peak voltage of the output side to meet the operation condition in (11).

Figure 13 shows the harmonic analysis result of the input current ripple component in 200 V_{dc} input voltage condition of the proposed converter. The double-line frequency power ripple component as a 100 Hz on the input current is normalized by each DC component of the input current. As the analysis result, the double-line frequency ripple component on the input current is reduced by 84.5% compared without the active power decoupling method.

Figure 14 depicts the characteristic of the ripple component within the output power from 200 W to 2.0 kW. Note that the

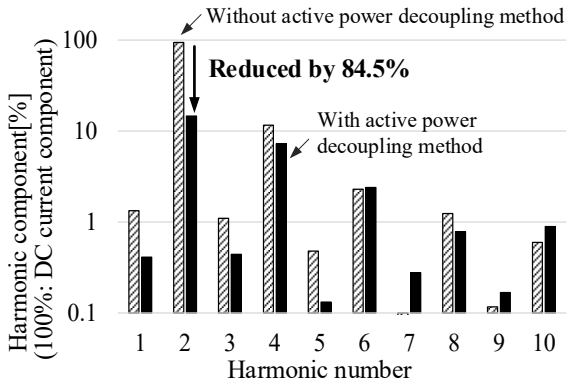


Fig. 13 Harmonic analysis result when output power is 1 kW with the condition as shown in Table 1. The 2nd order harmonic of 100 Hz component is reduced by 84.5% by proposed converter and the active power decoupling method.

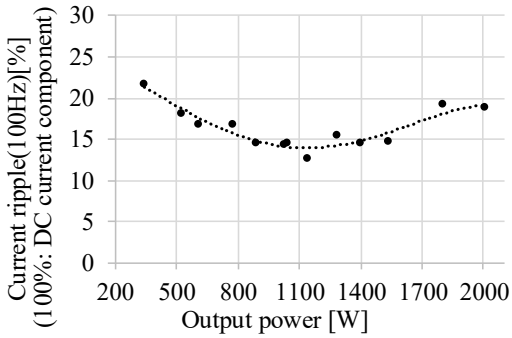


Fig. 14 Characteristic of ripple component on input current within output power from 200 W to 2 kW. The harmonics results of the proposed converter are confirmed to the good active power decoupling capability, which is below 75.0% compered by without active power decoupling over entire power range.

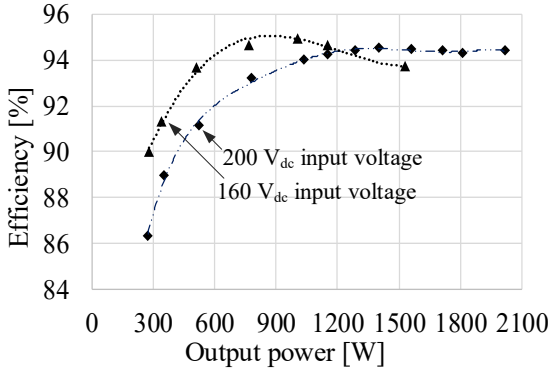


Fig. 15 Measured conversion efficiency of proposed converter with active power decoupling operation.

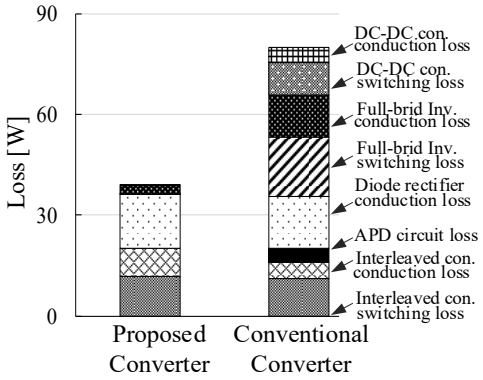


Fig. 16 Converter loss analysis with active power decoupling operation at rated output power of 2 kW. In the proposed converter, the switching loss of the secondary inverter is almost zero, because it is operated at the twice grid frequency.

characteristic shows the experimental results with the proposed active power decoupling method under the condition in Table 1. This double-line frequency power ripple component (100 Hz) on the input current was experimental results by applying the active power decoupling method. From the analysis result, the double-line frequency power ripple component was reduced by 87.6% compared without the active power decoupling operation in maximum. This is attributed that the power pulsation is compensated by the active power decoupling operation.

Figure 15 depicts the power conversion efficiency of the experiment setup as shown in Table 1. The configuration of these efficiency characteristic is result, which includes the active power decoupling operation. The input voltage is 160 V_{dc} and 200 V_{dc}. The maximum efficiency with an input voltage condition of 200 V_{dc} reaches 94.5% at 1410 W in the propose converter. Note that the maximum efficiency with the low input voltage condition is 95.0% because this condition has the lower core loss of the coupled inductor and snubber loss than that with the 200-V_{dc} operation. The efficiency improvement is from the reduction in applied voltage to the coupled inductor and the snubber circuit. As an experimental result, it is confirmed that the proposed converter under the low voltage condition has a loss, which is 32.2% lower than that under the 200-V_{dc} condition.

Figure 16 shows the loss analysis of the semiconductor elements at the rated power of each converter. The same semiconductor elements and the switching frequency are used as the analysis conditions, which compare the conventional active power decoupling topology as shown in Fig. 2. From analysis result, the total loss of the proposed converter is 48.1% lower in comparison with that of the conventional converter in Fig. 2. In the proposed converter, the arm current rms value of the primary converter due to the compensated operation of the buffer capacitor is increased or decreased, so the total conduction loss of the proposed interleaved converter increases. However, the total conduction loss of the proposed interleaved converter with the active power decoupling capability is almost the same the conventional interleaved converter with APD circuit. It is note that the switching loss of secondary inverter in the proposed converter is almost zero. The efficiency improvement of the proposed converter will be achieved by reducing the conduction loss of the diode rectifier, which is changing to a synchronous rectifier operation equipped with the switching devices.

6. Conclusion

This paper proposes a novel active power decoupling circuit that is integrated with an interleaved boost converter for isolated DC to single-phase AC conversion applications. The proposed converter is controlled to the power conversion and the active power decoupling operation independently by common-mode operation of the interleaved inverter. Therefore, in the proposed method the additional switching devices and the magnetic components for the

active power decoupling operation do not required to employ the coupled inductor. The performance of the proposed isolated converter is demonstrated by the experimental result in order to confirmed the validify of the proposed method. As the experimental results, the second-order harmonic due to the ripple component of the dc input current is reduced by 84.5% owing to the active power decoupling capability. Moreover, the proposed isolated converter has realized the maximum efficiency of 94.5%.

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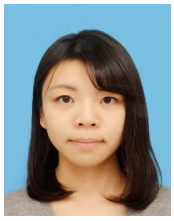

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