Intra-arm Balancing Control of Cascaded Multi-Port Converter for Whole Power Unbalance Conditions

Takumi Yasuda and Jun-ichi Itoh
NAGAOKA UNIVERSITY OF TECHNOLOGY
1603-1, Kamitomioka-machi, Nagaoka, Niigata, Japan
Tel.: +81 / (258) – 47.9533.
E-Mail: t_yasuda@stn.nagaokaut.ac.jp, itoh@vos.nagaokaut.ac.jp
URL: http://itohserver01.nagaokaut.ac.jp/itohlab/en/index.html

Keywords

«Modular Multilevel Converters (MMC)», «Load imbalance», «Capacitor voltage balancing», «AC-DC converter», «Charging infrastructure for EV´s»

Abstract

This paper proposes a capacitor voltage balancing control for load imbalance among cells in a cascaded multi-port converter. The input/output power of the cell is controlled by adjusting the ac-side voltage of the cell to balance the capacitor voltage even when the load imbalance occurs in the arm. The current of the multi-port converter with the conventional controller can distort due to overmodulation of the cell under the large load imbalance. The proposed controller prevents overmodulation with the improved generation method of the ac-side voltage, which extends the operation region with respect to the power imbalance. Furthermore, the proposed controller injects minimal additional circulating current to achieve the operation for whole power conditions. The experimental results reveal that the proposed controller improves the total harmonic distortion of the grid current by 2.9p.t. with minimal circulating current while achieving the capacitor voltage balancing.

Introduction

Recently, cascaded multi-port converters have been actively researched as a decentralized battery energy storage system [1]-[6], an integrated PV power conditioner [7]-[10], and so on [11], [12]. The cascaded configuration of cells realizes a grid connection without a bulky line frequency transformer [13], [14]. In addition, a filter on the ac-side is downsized due to the multilevel operation compared to conventional 2-level converters [2], [15].

Fig. 1 shows a cascaded multi-port converter. The multi-port converter in this paper is composed of the cascaded chopper cells and has no high-voltage dc-link port. The loads, such as the battery and EV, are assumed to be connected in parallel to the cell capacitor. Although the rated voltage and power of the cells are identical, a power imbalance among the cells can appear due to the different operation points of the loads caused by factors such as a slight difference in parasitic parameters and operating environments. The balancing controller of the multi-port converter is required to balance the capacitor voltage of the cells in spite of the power imbalance. In other words, the controller for the multi-port converter distributes the different

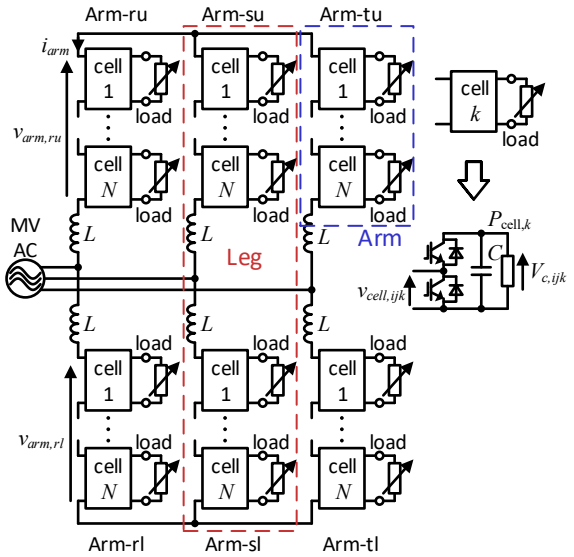


Fig. 1. Multi-port converter using modular multilevel cascaded converter with double-star chopper cells.

amounts of power to each cell according to the states of the load.

A circulating current is utilized to interact the power between the arms when a power imbalance occurs among the arms [4], [12]. Besides, a different ac-side voltage of each cell is applied to distribute the desired power when loads of cells within the arm are not identical. However, there is an operational limit with respect to the power imbalance because the ac-side voltage of the cells has to avoid overmodulation to suppress current distortion [5]-[8]. The additional circulating current (intra-arm balancing current) prevents the overmodulation because the larger arm current reduces the required amplitude of the ac-side voltage of the cell to gain the desired power. However, the past literature seems that the intra-arm balancing current controllers have not been proposed with a discussion of a hardware design of the multi-port converter, including the intra-arm balancing current effect.

This paper proposes an intra-arm balancing controller for the multi-port converter with a bidirectional operation, which operates in all possible power conditions with the compensation voltage injection to the ac-side voltage of the cell and the intra-arm balancing current control. The proposed controller minimizes the intra-arm balancing current while balancing all the capacitor voltage in the converter. In addition, the cell of the converter is designed to achieve the operation in whole power conditions taking into account the effect of the intra-arm balancing current. This paper is organized as follows; first, the control strategy for the multi-port converter is proposed. Next, the multi-port converter is designed. Finally, the proposed controller is evaluated by the simulation and the experiment with a miniature model. The experimental results show that the proposed controller prevents the overmodulation of the cells by the minimal intra-arm balancing current and improves the total harmonic distortion (THD) compared with the conventional controller. Moreover, the intra-arm balancing current is minimized by the proposed controller.

Controllers for multi-port converter

The objectives of the controller for the multi-port converter are to shape the grid current and to balance all the cell capacitor voltage in spite of the load imbalance among the cells. In order to achieve that, the balancing controllers are installed to distribute a different amount of power among the cells.

In this paper, a voltage redundancy ρ is defined as a ratio of the peak-to-peak value of the grid phase voltage to the maximum available voltage of the arm in the steady-state as

$$\rho := \frac{NV_c}{2\sqrt{2}V_g} \tag{1}$$

where N is the number of cells in one arm, V_c is the capacitor voltage of the cell, and V_g is the RMS value of the grid phase voltage.

Current controllers and inter-arm balancing controllers

Fig. 2 depicts the proposed control block diagram for the multi-port converter. The grid-side controller controls the average capacitor voltage in the converter by controlling the input and output power of the converter and shapes the grid current. The power is distributed evenly to each cell by the grid-side controller. The balancing controllers redistribute the power to the cells according to the state

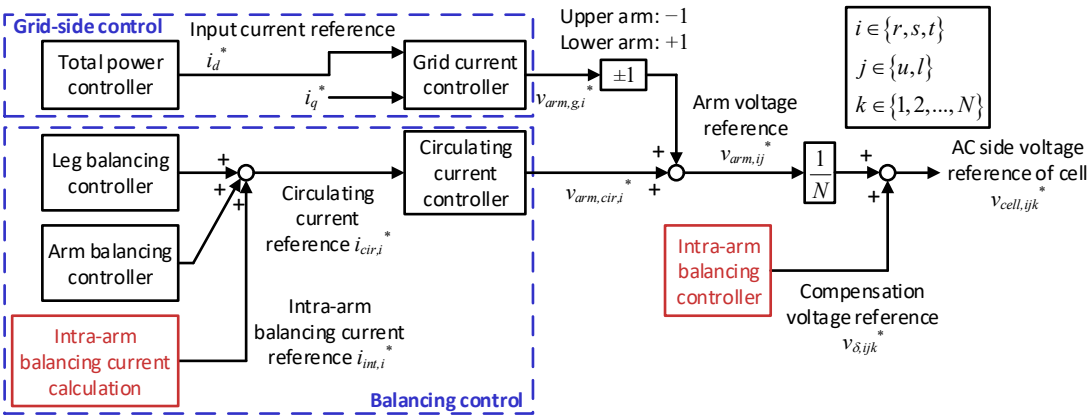


Fig. 2. Proposed control strategy of multi-port converter

of the loads in order to control all the capacitor voltages of the cells to the command value. The leg balancing controller regulates the averaged capacitor voltage of the phase by the power distribution utilizing a dc circulating current. The arm balancing controller utilizes the circulating current of the fundamental frequency to interchange the power between the upper and lower arm. The proposed intra-arm balancing current calculation block generates the intra-arm balancing current command, which is explained in detail in the following subsection. A sum of the output of the grid current controller and the circulating current controller is the arm voltage reference, which is assumed as

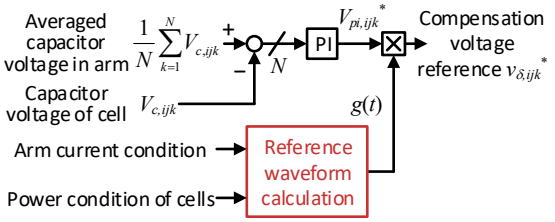


Fig. 3. Block diagram of proposed intra-arm balancing controller with optimized reference waveform.

$$v_{arm,ij}(t) = \frac{NV_c}{2} - K_j\sqrt{2}V_g\cos\left(\omega_g t - \phi_i\right) \quad \ldots\left(i \in \{r,s,t\},\, j \in \{u,l\}\right) \tag{2}$$

where K_u=1, K_l=−1, ω_g is the angular grid frequency, ϕ_i is the phase angle (ϕ_r=0, ϕ_s=2π/3, ϕ_t=4π/3). Note that (2) neglects the voltage drop on the arm inductor L. This paper defines the arm current as

$$i_{arm,ij}(t) \coloneqq I_{0,i} + \sqrt{2}I_{1,ij}\cos\left(\omega_g t - \phi_{1,ij} - \phi_i\right) + i_{int,i}(t) \tag{3}$$

where $I_{0,i}$ is the dc circulating current of phase i, $I_{1,ij}$ and $\phi_{1,ij}$ is the RMS value and the phase angle of the fundamental frequency component of the arm current, respectively, which is the sum of the grid current and the circulating current for the upper/lower arm balancing, and $i_{int,i}$ is the intra-arm balancing current. Since there is no high-voltage dc-link port in the multi-port converter, as shown in Fig. 1, the circulating current circulates through three phase legs. Thus, the circulating current of the three phases can be different when a power imbalance occurs among the cells.

The sum of the arm voltage reference and the compensation voltage from the proposed intra-arm balancing controller is the ac-side voltage reference of the cells. This paper adopts the phase-shifted PWM (PS-PWM), which is suitable for decentralized control [16], [17].

Intra-arm balancing controller

The intra-arm balancing controller regulates the capacitor voltage error among the cells within the arm by injecting the compensation voltage to the ac-side voltage reference of the cells.

Fig. 3 shows the proposed intra-arm balancing controller. The controller feedbacks the capacitor voltage and regulates the capacitor voltage deviation within the arm to zero. The reference waveform is obtained by multiplying a reference waveform $g(t)$ to an output by the PI controller. Since the command of the intra-arm balancing controller is the averaged capacitor voltage of the cell within the arm, the sum of the outputs of the PI controllers over the arm is always zero, that is,

$$\sum_{k=1}^{N} v_{\delta,ijk}^{*}(t) = g(t)\sum_{k=1}^{N} V_{pi,ijk}^{*} = 0\,. \tag{4}$$

Eq. (4) implies that the arm voltage, which is the sum of the ac-side voltage of the cells in the arm, is not affected by the compensation voltage regardless of any selection of the reference waveform $g(t)$. Therefore, $g(t)$ is designed to guarantee the operation without the overmodulation over wide power conditions. The boundary of the overmodulation for the compensation voltage is expressed as

$$-\frac{v_{arm,ij}(t)}{N} \le v_{\delta,ijk}(t) \le V_{c,ijk} - \frac{v_{arm,ij}(t)}{N}\,. \tag{5}$$

The maximum amplitude of the compensation voltage is calculated from the arm voltage reference and the capacitor voltage. Besides, the compensation power $P_{\delta,ijk}$, which is the power obtained by the compensation voltage, is calculated as

$$P_{\delta,ijk} = \frac{1}{T_g}\int_0^{T_g} v_{\delta,ijk}(t)\,i_{arm,ij}(t)\,dt \tag{6}$$

where T_g is a fundamental period. Here, a maximum and minimum compensation power $P_{\delta,ij,max}$ and $P_{\delta,ij,min}$ are defined as a maximum and a minimum power in arm-ij which is generated by the intra-arm balancing controller without the overmodulation with an arbitrary reference waveform $g(t)$, respectively.

In order to prevent diverging the capacitor voltage, the intra-arm balancing controller has to satisfy

$$P_{\delta,ij,min} \le \min_k \left[P_{cell,ijk} - \frac{1}{N}\sum_{k=1}^{N} P_{cell,ijk} \right], \quad P_{\delta,ij,max} \ge \max_k \left[P_{cell,ijk} - \frac{1}{N}\sum_{k=1}^{N} P_{cell,ijk} \right]. \tag{7}$$

For example, the reference waveform $g(t)$ should be adjusted so that the $P_{\delta,ij,max}$ becomes large when there is a significantly heavier load on the cell than the typical load in the arm. On the other hand, $g(t)$ should be adjusted to decrease $P_{d,ij,min}$ for the significantly lighter load than the typical load. Therefore, $g(t)$ is decided by the loaded conditions of the cells in the arm as,

$$P_{\delta,ij,max} : P_{\delta,ij,min} = \max_k \left[P_{cell,ijk} - \frac{1}{N}\sum_{k=1}^{N} P_{cell,ijk} \right] : \min_k \left[P_{cell,ijk} - \frac{1}{N}\sum_{k=1}^{N} P_{cell,ijk} \right]. \tag{8}$$

The proposed intra-arm balancing controller calculates $g(t)$, fulfilling (5) and (8) online.

Fig. 4 shows an example of the ac-side voltage of the cell generated by the proposed intra-arm balancing controller. The voltage varies discontinuously according to the polarity of the arm current. The amplitude of the compensation voltage is decided from the instantaneous arm voltage reference.

The operation region with respect to the power imbalance is extended by the proposed intra-arm balancing controller with the optimized reference waveform. However, the capacitor voltage balance is not necessarily achieved in whole power conditions even though the proposed reference waveform is applied. For example, it is obvious that the compensation voltage does not contribute to the power distribution, and the capacitor voltage would diverge in the case of $i_{arm,ij}(t)=0$ as shown in (6). It means that the intra-arm balancing current is required under some conditions.

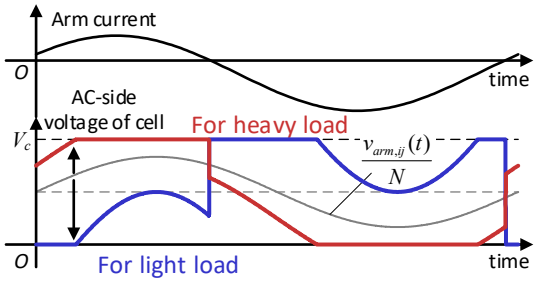


Fig.4. Example of the ac-side voltage reference of the cell with the compensation voltage reference. The loaded condition in the arm is that the magnitude of the maximum load imbalance in the arm is half of that of the minimum load imbalance in the arm.

Intra-arm balancing current calculation

The larger compensation power $P_{\delta,ij,max}$ and the smaller $P_{\delta,ij,min}$ reduce the possibility of overmodulation. The larger intra-arm balancing current increase $P_{\delta,ij,max}$ and decrease $P_{\delta,ij,min}$, which result in the extension of the operation region. However, the large intra-arm balancing current injection causes the large switching and conduction losses. Therefore, the proposed intra-arm balancing current calculation part in Fig. 2 minimizes the intra-arm balancing controller online to suppress the loss.

Fig. 5 shows the flowchart of the proposed intra-arm balancing current calculation. The controller minimizes the intra-arm balancing current in the steady-state. First, the proposed controller calculates the maximum and the minimum compensation power $P_{\delta,ij,max}$ and $P_{\delta,ij,min}$ from the arm current with the discrete integral. The arm current for the calculation is the command value generated by the other balancing controllers in this paper. Then, the controller minimizes the intra-arm balancing current with

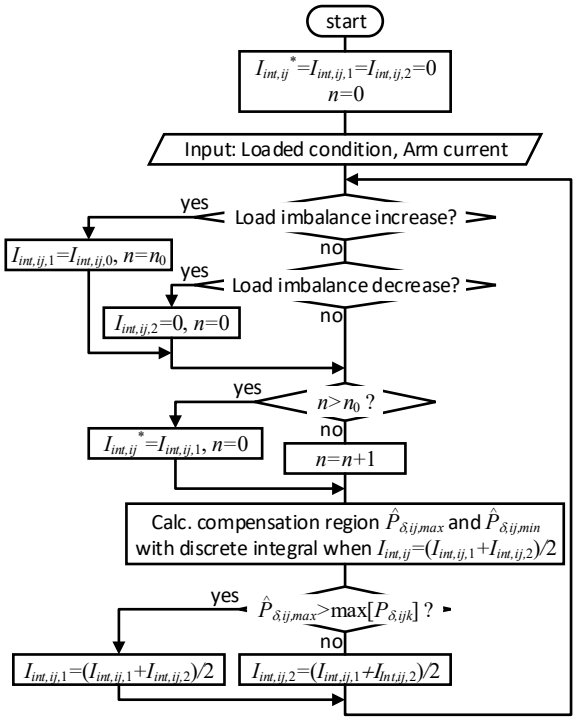


Fig. 5 Minimization strategy of intra-arm balancing current using bisection and discrete integral. The maximum value of derived $I_{int,ij}^{*}$ in six arms is applied to the converter as the intra-arm balancing current reference.

the bisection by comparing the calculated $P_{\delta ij,max}$ and $P_{\delta ij,min}$ to the loaded condition. The minimization is performed in each arm. Finally, the maximum value of the derived $I_{int,ij}^*$ for six arms is applied as the intra-arm balancing current I_{int}^*. The intra-arm balancing current $I_{int,ij}^*$ is only updated when the derived $I_{int,ij}$ satisfies (7) and is smaller than $I_{int,ij}^*$, which is the minimum intra-arm balancing current derived in the last calculation. An update frequency of the intra-arm balancing current reference is set to be sufficiently low not to interfere with the intra-arm balancing controller in Fig. 3. In addition, a low pass filter with a cut-off frequency of 6.7 Hz is installed on the output of the intra-arm balancing current calculation to prevent a step change of the current reference. In this paper, the intra-arm balancing current reference input to the circulating current controller is 1.1 times larger than the derived value considering the calculation error because the proposed algorithm works as a feed-forward controller.

$I_{int,ij}^*$ is increased temporarily to a sufficiently large value $I_{int,0}$ to satisfy (7) when the power imbalance increases as a result of the load variation. In this paper, $I_{int,0}$ is decided from the rated current of the system and the given arm current condition as

$$I_{int,ij,0} = \sqrt{{I_{arm,n}}^2 - \left({I_{0,i}}^2 + {I_{1,ij}}^2\right)} \tag{9}$$

where $I_{arm,n}$ is a rated current of the arm. The multi-port converter operates without the overmodulation with $I_{int,ij,0}$ in any loaded conditions if the rated current is designed properly, as in the following section. The initial interval of the bisection is set to $I_{int,ij,0}$ and $I_{int,ij}^*$, which are (9) and the minimum intra-arm balancing current derived by the last calculation, respectively. The amplitude of the intra-arm balancing current can be decreased. Thus, the bisection interval is changed to $I_{int,ij}^*$ and zero when the power imbalance decreases due to the load variation. Note that this paper assumes that the controller can detect the loaded condition. This is because the applications of the multi-port converter are the integrated PV power conditioner and the battery energy storage system, which usually measures the load voltage and the current to perform the maximum power point tracking or control a state-of-charge.

The frequency of the intra-arm balancing current I_{int} has to be chosen not to interfere with other controllers. Too low frequency of I_{int} increases the capacitor voltage ripple [18], [19]. On the other hand, too high frequency of I_{int} increases the voltage drop on the arm inductor, which may result in the saturation of the arm voltage. Therefore, this paper adopts the double-frequency component as I_{int} as

$$i_{int,i}(t) := -\sqrt{2} I_{int} \sin\left(2\omega_g t - 2\phi_i\right). \tag{10}$$

Note that the phase angle (10) is based on (2).

Fig. 6 compares the intra-arm balancing current I_{int} required to operate in the power imbalance. The conventional controller in Fig. 6 utilizes the polarity of the arm current as the reference waveform $g(t)$ [3], [4]. Required I_{int} becomes larger as the load imbalance increases. The proposed controller reduces the intra-arm balancing current compared to the conventional controller. It reveals that the proposed intra-arm balancing controller helps to reduce the arm current of the converter.

Design of switching devices and cell capacitors

In this section, the switching devices and the cell capacitors are designed considering the intra-arm balancing. As described above, the intra-arm balancing current is derived by the nonlinear calculation with the discrete integral and the bisection. Therefore, this section presents the maximum arm current of the converter with the proposed controller calculated numerically. 64 million loaded conditions were analyzed.

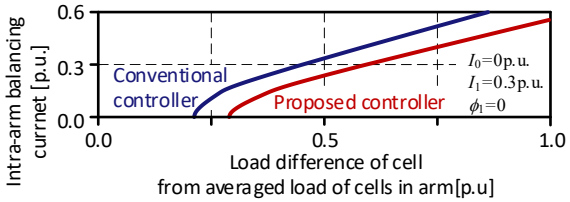


Fig. 6. Comparison of required intra-arm balancing current for operation in a power imbalance. The magnitude of the minimum load difference is set to double that of the maximum load difference. The intra-arm balancing current and the power imbalance are normalized by the rated grid current and the averaged power of cells in the arm, respectively.

Fig. 7 shows the maximum intra-arm balancing current and the maximum arm current of the system, which is derived as a result of the numerical calculation. The current is normalized by the rated grid current. The maximum intra-arm balancing current decrease as the voltage redundancy ρ, which is defined in (1), increases. Since the large ρ allows the cell to inject a larger

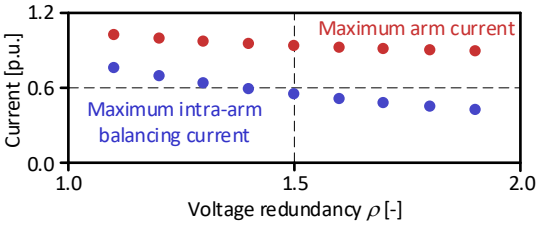


Fig. 7. Maximum intra-arm balancing current and arm current.

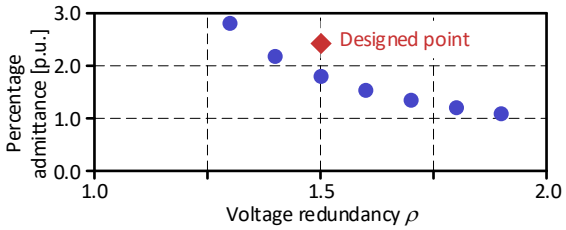


Fig. 8. Minimum capacitance for operation without overmodulation.

amplitude of the compensation voltage, the required amplitude of the intra-arm balancing current decreases. As a result, the maximum arm current is reduced. Fig. 7 reveals that almost double arm current in the full loaded operation is required for the system when ρ=1.5, which is the condition in the following simulation and experiment. $I_{arm,n}$ in (9) is designed as 0.94 times as rated grid current.

Fig. 8 shows the minimum capacitance to avoid the overmodulation in whole power conditions. The required capacitance decreases as ρ increases. Since the maximum arm current is reduced by the large ρ, the capacitor voltage ripple is reduced as ρ increases. In addition, the cell can operate without the overmodulation even though the capacitor voltage contains larger fluctuation when ρ is large. Practically, the cell capacitance is required to be designed with redundancy. The indication written as "Designed point" in Fig. 8 indicates a cell capacitance for the simulation and the experiment in the following section.

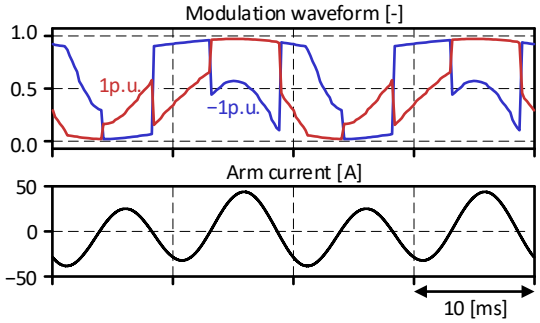
Simulation results

Table I shows the simulation conditions. In this simulation, both the cell with the power of 1p.u. and the cell with the power of −1p.u. are in the same arm, which is the largest power imbalance for the converter. One calculation of the discrete integral in Fig. 5 is performed every 1 ms, and the update frequency of the intra-arm balancing current command is set to 6.7 Hz, which is also applied to the practical controller.

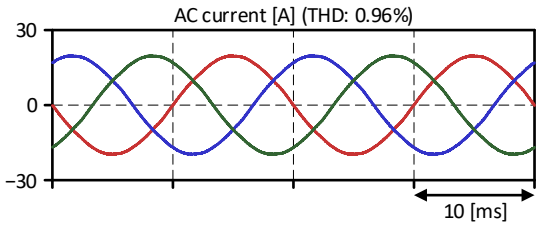
Fig. 9 shows the simulation results of the steady-state operation with the load imbalance. Fig. 9(a) shows modulation waveforms of the cells and the arm current in the corresponding arm. The proposed controller injects different compensation voltages. A large second harmonic component of 20.8 A is injected as the intra-arm balancing current i_{int} in order to operate in the severe power imbalance, which is 13.4% larger than the theoretical minimum value. The calculation error is 3.4% because a 10% larger i_{int} of the originally derived value by the controller is applied to the system, as mentioned above. The error is caused by the error between the current used for the calculation in the proposed controller and the true value. Fig. 9(b) shows the grid current. The converter operates with a THD of

Table I. Simulation conditions

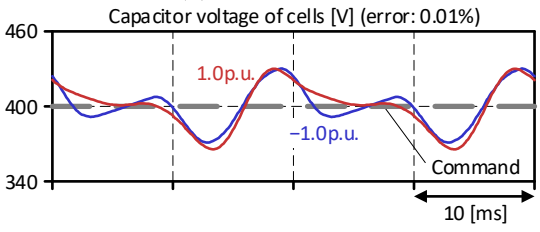
Parameter	Symbol	Value
Rated power of cell	P_{cell}	2.2 kW
Grid line-line voltage	$\sqrt{3}V_g$	6.6 kV (RMS)
Grid frequency	f_g	50 Hz
Number of cells per arm	N	40
Rated capacitor voltage	V_c	400 V
Arm inductance	L	158 mH (0.10p.u.)
Cell capacitance	C	1.87 mF (68 mJ/VA)
Carrier frequency	f_{car}	6.0 kHz



(a) Modulation waveforms and arm current of upper arm in r-phase.



(b) Grid current



(c) Capacitor voltage of cells.

Fig. 9. Simulation results of steady-state operation with load imbalance.

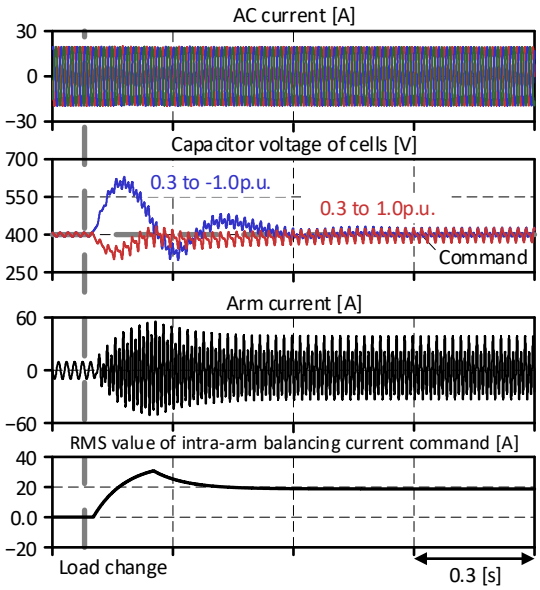


Fig. 10. Simulation result of transient response under step increase of load imbalance.

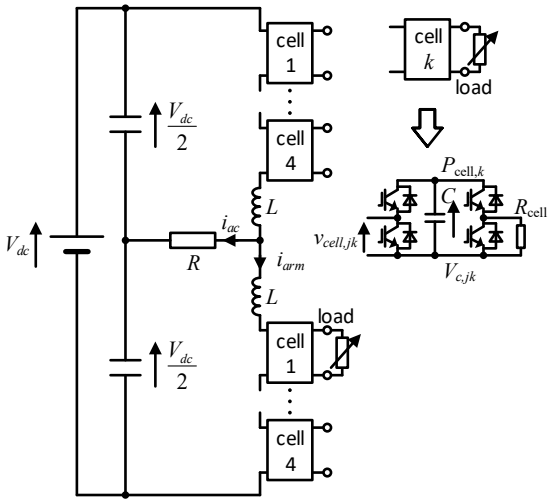


Fig. 11. Scaled model for experimental verification of proposed intra-arm balancing controller.

0.96% despite the largest power imbalance. Fig. 9(c) shows the capacitor voltages of the cells in the same arm. The capacitor voltages are balanced thanks to the proposed controller.

Fig. 10 shows the transient response under the load variation. Before the load change, there is no power imbalance in the arm and no intra-arm balancing current i_{int} flows. After the load change, one cell is fully loaded, and a load of another cell becomes −1p.u. The command of i_{int} increases rapidly after the load change. Then, i_{int} is decreased thanks to the proposed controller. The capacitor voltage of the cells and the grid current is balanced.

Table II. Experimental conditions.

Parameter	Symbol	Value
Rated power of cell	P_{cell}	169 W (R_{cell}=100 Ω)
AC line-line voltage	$\sqrt{3}V_g$	125 V (RMS)
DC-link voltage	V_{dc}	520 V
Grid frequency	f_g	50 Hz
Number of cells per arm	N	4
Rated capacitor voltage	V_c	130 V
AC resistance	R	50 Ω
Arm inductance	L	5.0 mH (0.07p.u.)
Cell capacitance	C	1.36 mF (68 mJ/VA)
Carrier frequency	f_{car}	6.0 kHz

Experimental results

Fig. 11 and Table II show the experimental circuit and the conditions. The experimental multi-port converter is composed of single-phase cascaded choppers, and the dc voltage source is utilized instead of the other two phases. The variable load is installed in only one cell to emulate the condition that there is a fully loaded cell and an unloaded cell in the same arm.

Fig. 12 shows the block diagram of the controller for the experiment. The output of the total power controller is dc circulating current command, unlike Fig. 2. The grid current is controlled at a constant value of I_d=2.5 A and I_q=0 A to keep the voltage redundancy ρ constant. The proposed controller was tested under the condition that the dc and the fundamental frequency component of the arm current flow.

Fig. 13 shows experimental waveforms in the steady-state operation with the power imbalance when the proposed controller is applied. The different modulation waveforms and the relatively large intra-arm balancing current i_{int} of 1.93 A are applied, as shown in Fig. 13(a). The error of i_{int} from the theoretical minimum value is 2.38%. Fig. 13(b) shows the grid current with a THD of 3.98% even under the power imbalance. The capacitor voltage is balanced with a maximum error of 1.3% as in Fig. 13(c).

Fig. 14 shows experimental waveforms in the steady-state operation with the power imbalance when the conventional controller [3], [4] is adopted. The conventional controller does not inject the i_{int}. The overmodulation occurs in the cells on account of the large amplitude of the compensation voltage by the conventional intra-arm balancing controller. As a result, the arm current and the grid current distort. THD of the grid current deteriorates by 2.9p.t. compared with the proposed controller.

Fig. 15 shows the transient behavior of the converter with the proposed controller when the load in

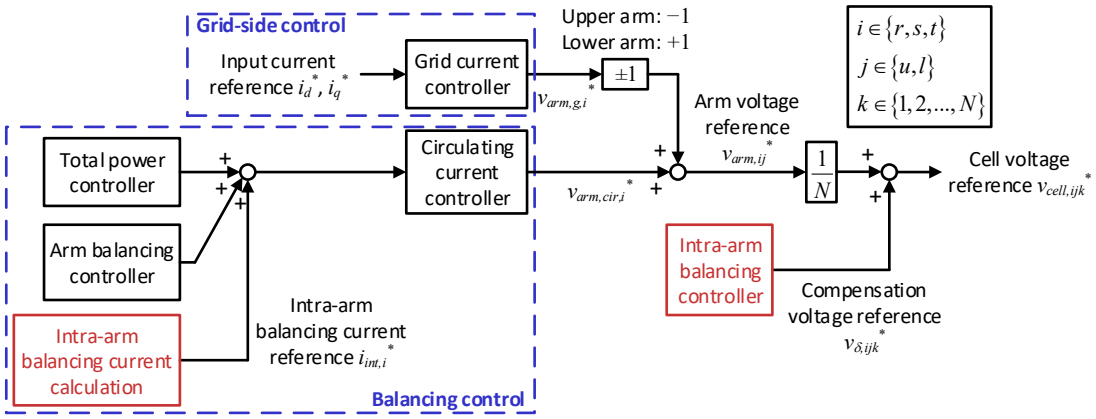
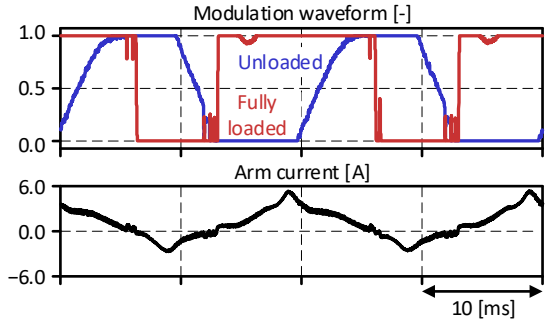
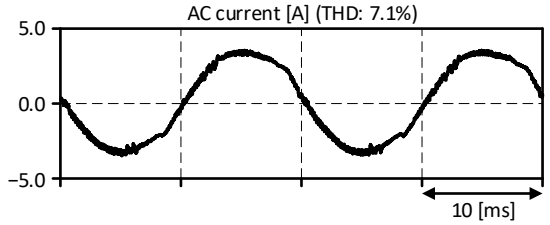


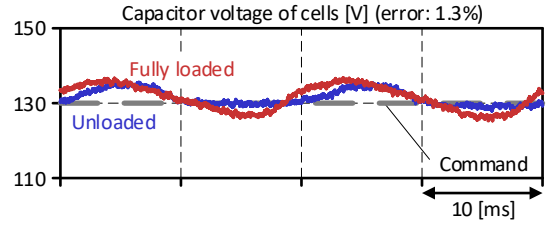
Fig. 12. Control strategy for experimental circuit.



(a) Modulation waveforms and arm current of upper arm in r-phase.

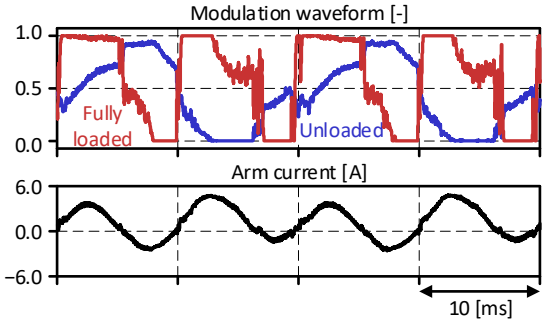


(b) Grid current.

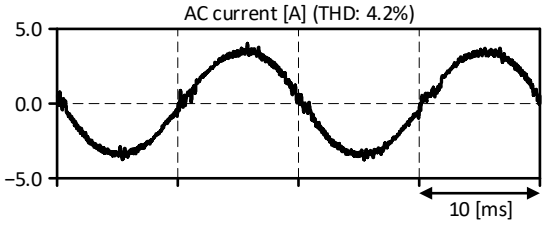


(c) Capacitor voltage of cells.

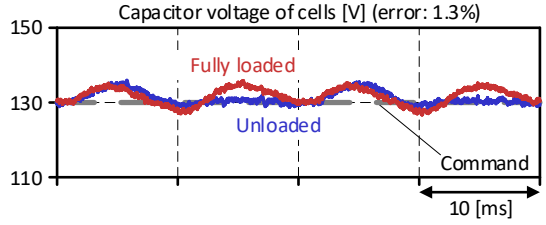
Fig. 14. Experimental results of steady-state operation with conventional controller in load imbalance.



(a) Modulation waveforms and arm current of upper arm in r-phase.



(b) Grid current.



(c) Capacitor voltage of cells.

Fig. 13. Experimental results of steady-state operation with proposed controller in load imbalance.

one cell increases from 0p.u. to 1p.u. The proposed controller decreases i_{int} and converges to 2.21 A, which is 11% larger than the theoretical minimum value, although i_{int} increases after the load variation. The capacitor voltage drops by approximately 30% of its nominal value after the load change. After that, the capacitor voltage converges to the command value of 130 V within 1 s. The update of i_{int} causes a small voltage drop of 12% on the cell capacitor at 0.15 s after the load change. However, the voltage fluctuation on the cell capacitor does not affect the grid current.

Fig. 16 shows the transient response when the load in one cell increases from 1p.u. to 0.5p.u. i_{int} decreases to zero after the load changes, and the power imbalance in the arm decreases. The capacitor voltage increases by 23% at maximum after the load change. The capacitor voltage converges to the command value within 0.5 s, even though the change of i_{int} causes the overshoot of the voltage. The grid

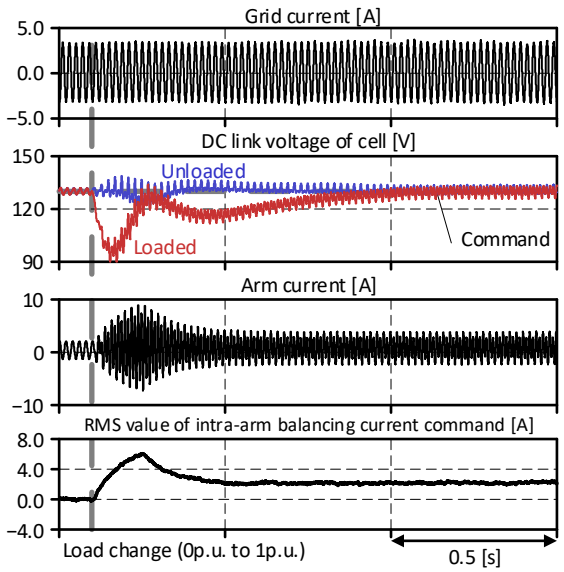


Fig. 15. Experimental results of transient behavior under step increase of load imbalance.

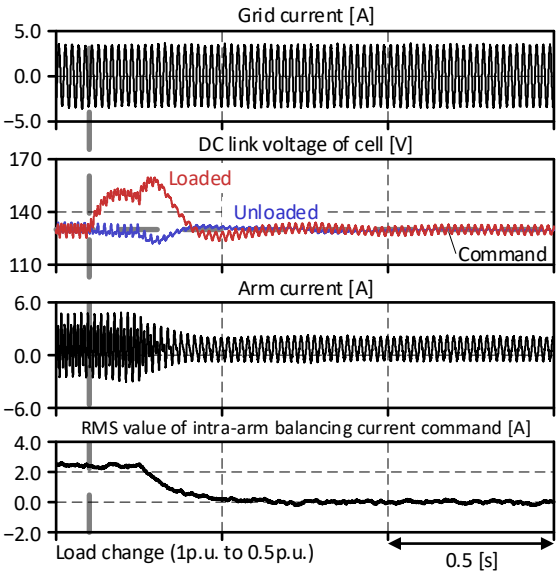


Fig. 16. Experimental results of transient behavior under step decrease of load imbalance.

current is little affected by the load variation. These results verify that the proposed controller achieves operation in whole power conditions with the minimum intra-arm balancing current.

Conclusion

This paper proposed the intra-arm balancing controller to achieve the capacitor voltage balancing under the power imbalance with the minimum current injection. In addition, the maximum arm current and the cell capacitors were designed to ensure the operation in all power conditions considering the effect of the intra-arm balancing current. The experimental result with the designed multi-port converter achieved both the balanced grid current and the balanced capacitor voltages of all cells. The proposed controller improved the grid current THD by 2.9pt compared with that of the conventional controller. In addition, the intra-arm balancing current was minimized with an error of 2.38% compared with the theoretical minimum current.

References

[1] N. Kawakami, S. Ota, H. Kon, S. Konno, H. Akagi, H. Kobayashi, and N. Okada, "Development of a 500-kW Modular Multilevel Cascade Converter for Battery Energy Storage Systems," in IEEE Transactions on Industry Applications, vol. 50, no. 6, pp. 3902-3910, Nov.-Dec. 2014.

[2] G. Wang et al., "A Review of Power Electronics for Grid Connection of Utility-Scale Battery Energy Storage Systems," in IEEE Transactions on Sustainable Energy, vol. 7, no. 4, pp. 1778-1790, Oct. 2016.

[3] Z. Wang, H. Lin, Y. Ma and T. Wang, "A prototype of modular multilevel converter with integrated battery energy storage," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 434-439.

[4] W. Zeng, R. Li and X. Cai, "A New Hybrid Modular Multilevel Converter with Integrated Energy Storage," in IEEE Access, vol. 7, pp. 172981-172993, 2019.

[5] T. Soong and P. W. Lehn, "Assessment of Fault Tolerance in Modular Multilevel Converters With Integrated Energy Storage," in IEEE Transactions on Power Electronics, vol. 31, no. 6, pp. 4085-4095, June 2016.

[6] G. Liang et al., "Analytical Derivation of Intersubmodule Active Power Disparity Limits in Modular Multilevel Converter-Based Battery Energy Storage Systems," in IEEE Transactions on Power Electronics, vol. 36, no. 3, pp. 2864-2874, March 2021.

[7] S. Yang et al., "Quantitative Comparison and Analysis of Different Power Routing Methods for Single-Phase Cascaded H-Bridge Photovoltaic Grid-Connected Inverter," in IEEE Transactions on Power Electronics, vol. 36, no. 4, pp. 4134-4152, April 2021.

[8] P. Sochor and H. Akagi, "Theoretical and Experimental Comparison Between Phase-Shifted PWM and Level-Shifted PWM in a Modular Multilevel SDBC Inverter for Utility-Scale Photovoltaic Applications," in

IEEE Transactions on Industry Applications, vol. 53, no. 5, pp. 4695-4707, Sept.-Oct. 2017.

[9] L. Liu, H. Li, Y. Xue and W. Liu, "Reactive Power Compensation and Optimization Strategy for Grid-Interactive Cascaded Photovoltaic Systems," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 188-202, Jan. 2015.

[10] V. Sridhar and S. Umashankar, "A Comprehensive Review on CHB MLI based PV Inverter and Feasibility Study of CHB MLI based PV-STATCOM," in Renewable and Sustainable Energy Reviews, vol. 78, pp. 138-156, Oct. 2017.

[11] Y. Su, P. Wu and P. Cheng, "Design and Evaluation of a Control Scheme for the Hybrid Cascaded Converter in Grid Applications," in IEEE Transactions on Power Electronics, vol. 35, no. 3, pp. 3139-3147, March 2020.

[12] G. Guidi, S. D'Arco, K. Nishikawa and J. A. Suul, "Load Balancing of a Modular Multilevel Grid-Interface Converter for Transformer-Less Large-Scale Wireless Electric Vehicle Charging Infrastructure," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 4, pp. 4587-4605, Aug. 2021.

[13] J. Sastry, P. Bakas, H. Kim, L. Wang, and A. Marinopoulos, "Evaluation of Cascaded H-Bridge Inverter for Utility-Scale Photovoltaic Systems," in Renewable Energy, vol. 69, pp. 208-218, Sept. 2014.

[14] S. Alotaibi and Ahmed Darwith, "Modular Multilevel Converter for Large-Scale Grid-Connected Photovoltaic Systems: A Review," in Energies, vol. 14, p. 6213, Sept. 2021.

[15] Y. Zhong, N. Roscoe, D. Holliday, T. C. Lim and S. J. Finney, "High-Efficiency mosfet-Based MMC Design for LVDC Distribution Systems," in IEEE Transactions on Industry Applications, vol. 54, no. 1, pp. 321-334, Jan.-Feb. 2018.

[16] S. Yang, Y. Tang and P. Wang, "Distributed Control for a Modular Multilevel Converter," in IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5578-5591, July 2018.

[17] B. Çiftçi, S. Schiessl, J. Gross, L. Harnefors, S. Norrga and H. -P. Nee, "Wireless Control of Modular Multilevel Converter Submodules," in IEEE Transactions on Power Electronics, vol. 36, no. 7, pp. 8439-8453, July 2021.

[18] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist and H. Nee, "Dynamic Analysis of Modular Multilevel Converters," in IEEE Transactions on Industrial Electronics, vol. 60, no. 7, pp. 2526-2537, July 2013

[19] H. Fujita, M. Hagiwara, and H. Akagi, "Power Flow Analysis and DC-Capacitor Voltage Regulation for the MMCC-DSCC," in Electrical Engineering in Japan, vol. 193, no. 1, pp. 1-9, 2015.