Series/Parallel Connection Method of DC-DC Transformer for Scalable Power Converter Systems using USPM

Takumi Iwamoto, Koki Yamanokuchi, Hiroki Watanabe and Jun-ichi Itoh
NAGAOKA UNIVERSITY OF TECHNOLOGY
1603-1, Kamitomioka-machi, Nagaoka, Niigata, Japan
Tel.: +81 / (258) – 47.9533.
E-Mail: s225057@stn.nagaokaut.ac.jp, koki_yamanokuchi@stn.nagaokaut.ac.jp, hwatanabe@vos.nagaokaut.ac.jp, itoh@vos.nagaokaut.ac.jp
URL: http://itohserver01.nagaokaut.ac.jp/itohlab/jp/index.html

Acknowledgments

This work was supported by the Council for Science, Technology, and Innovation (CSTI), the Cross-ministerial Strategic Innovation Promotion Program (SIP), and "Energy systems of an Internet of Energy (IoE) society" (Funding agency: JST).

Keywords

«Dual Active Bridge Converter», «Circuit Control», «Parallel operation», «Series Operation».

Abstract

This paper proposes a series or parallel connection method of a DC-DC transformer (DCX) to achieve power scalability. Universal Smart Power Module (USPM) modularizes all power converter components. The power converter is realized by combining several USPMs to simplify the power electronics design. A USPM with galvanic isolation (isolated USPM) operates as a DCX. Isolated USPM must have high efficiency over a wide power range. In addition, the voltage or current must be balanced when connected in series or parallel. A dual-active-bridge converter is chosen as the main circuit for the isolated USPM for these requirements. The proposed method is demonstrated by an experimental setup. As a result, the current balance is improved by 75.0pt. in parallel connection, and the voltage balance is improved by 37.0pt. in series connection.

Introduction

In recent years, renewable energy applications and electric vehicles have been attracted from the viewpoint of carbon neutrality. Elemental technologies such as circuit topology, control methods, and design methods have been developed for various applications due to the increasing demand for such power converters. [1-3]. The development of the power converters requires specialized and multifaceted know-how such as circuit design, software development, and heat dissipation. Therefore, the development takes a large amount of time and costs. In order to adapt to the increasing demand for power converters in the future, the power converters need to be developed quickly and at a low cost.

Power conversion systems based on modular structures, such as Power Electronics Building Block (PEBB), are being considered to solve this problem [4-6]. A PEBB realizes a power conversion system by combining several modules, which contain main circuits designed for high power density. The PEBB eliminates the need to design the main circuit and reduces development time. These systems are scalable to adapt to various specifications by changing the number of modules. In case of failure, the system is easy to maintain as the modules only need to be replaced. However, a controller and noise filter must be developed separately, even though the main circuit and some auxiliary circuits are modularized. These developments require additional time and costs.

USPM has been proposed to further shorten development times and reduce costs for the PEBB concept [7-9]. The USPM modularizes not only the main circuit but also all components of the power converter, such as the controller and noise filter. The USPM allows any power conversion system to be built simply by combining USPMs. Therefore, the design of the power conversion system only requires the USPM selection, which greatly reduces the development speed. In the power conversion system using USPM, a single master controller controls many USPMs, and

each USPM operates independently and is decentralized. The behavior of each USPM is an ideal controllable voltage or current source. The USPM responds quickly to commands from the master controller to achieve power conversion. Furthermore, the USPM can be applied to high-voltage and high-current systems because it can be connected in multiple series and parallels.

The main circuits contained in the USPM are deployed in multiple configurations, such as single-phase H-bridges and three-phase inverters, to suit a wide range of applications. One of the various configurations is a USPM with galvanic isolation (isolated USPM). Isolated USPMs are required to behave like DC transformers that do not perform voltage conversion (always at a 1:1 voltage ratio) but only provide electrical isolation between the primary and secondary sides. In addition, it requires bidirectional power transfer and high-efficiency operation under a wide range of operating conditions. Isolated USPMs have not been studied with specific circuit schemes, whereas single-phase H-bridge USPMs have been studied in previous studies [7]. In addition, the control method for isolated USPMs in multi-serial and multi-parallel configurations has also not yet been studied.

This paper verifies the suitable topology and control methods for the isolated USPM. The new contribution of this paper is that the balancing method of the current or voltage for the parallel or serial connection is established. As a result, the series or parallel connection increases the voltage and current rating of a power converter system, respectively. In addition, the power balance of each USPM is kept with low bandwidth communication when multiple units are connected because the isolated USPM operates autonomously. This paper is organized as follows: First, isolated DC-DC converters are compared, and their features are summarized. Next, the control of isolated USPM is discussed. Finally, the effectiveness of the control method is verified through the verification of actual devices.

Universal Smart Power Module (USPM)

USPM in a power electronics system is similar to the integrated circuits (ICs) and operational amplifiers(Op-amps) in an electronics circuit. The USPM can construct a more complex power converter system. This is because the USPM has all the essential components of a power converter, such as the main circuits, noise

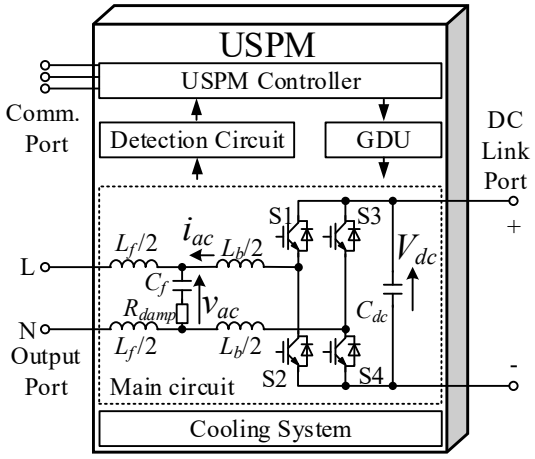


Fig. 1: Schematic diagram of USPM.

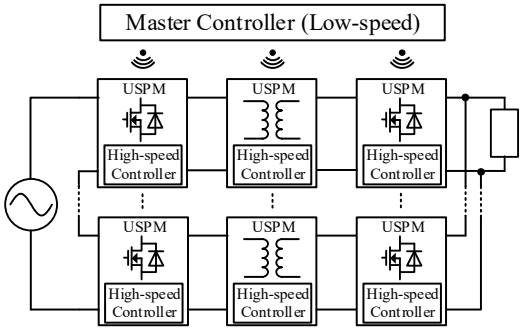


Fig. 2: Example of power conversion system using USPM.

filters, and high-speed controllers with communication. Therefore, designers of the power converter systems do not need the dedicated design of the main circuits, noise filters, and so on. As a result, The USPM achieves decreasing development time, reducing the design items, unnecessary designer's skills, and so on.

Fig. 1 shows one example of a USPM configuration with an H-bridge USPM. This module has the capability of AC-DC, DC-AC, and DC-DC conversion. The whole system will consist of several USPMs and a master controller for the entire power conversion system.

The USPM responds quickly to commands from the master controller by incorporating a noise filter and a high-speed controller in addition to the main circuit. Thus, the USPM works as an ideal controllable voltage or current source according to the command from the master controller. Communication cables among each USPM will be increased when USPM constructs the entire system. Wireless communications are used between the master and slave controllers in order to reduce the cables. It is difficult to control instantaneous values with a master controller

because the wireless communication speed is only a few tens of milliseconds at minimum. Thus, each USPM is controlled by sending an RMS value command from the master controller.

Fig. 2 shows a single-phase AC-AC power converter system as an example of a power conversion system using USPMs connected to an Input-Series-Output-Parallel (ISOP). USPM on the grid side is responsible for power factor correction (PFC) operation, while the USPM connected to the load side controls the load voltage.

The module used in the ISOP configuration requires galvanic isolation between the input and output because the different voltage potentials of USPMs are connected to each other. The power converter system using the galvanic isolation USPM has voltage and current sharing issues. Therefore, it is necessary to develop the USPM, which has the galvanic isolation capability, including the balance control for serial and/or parallel connection.

Circuit topology for isolated USPMs

The "isolated USPM" concept is a DC-DC transformer for the USPM-based power converter systems. In order to achieve the role, the isolated USPMs should have some functions and features as follows;

- Performing as a DC transformer with a voltage ratio of unity;
- High efficiency in a wide bidirectional output range;
- Adjustable current and/or voltage sharing function among parallel and/or series connected USPMs;

In this section, the suitable circuit topology is investigated in order to achieve these functions and features. Three major circuit configurations of the isolated DC-DC converter are selected as follows:

1. Phase-shifted full bridge DC-DC converter (PSFB) [10-11]
2. LLC converter [12-13]
3. Dual Active Bridge (DAB) converter [14-15]

Fig. 3 shows a PSFB DC-DC converter. The converter has inductor L_d, and the inductor current is controlled. The converter also performs as the buck chopper when the power flow is from the primary side to the secondary side. Thus, the voltage characteristic is changed by power flow. In addition, the inductor L_d must have a large

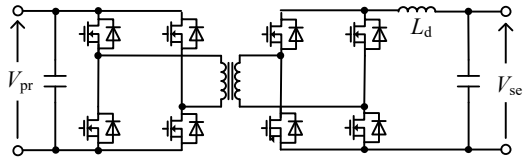


Fig. 3: Phase-shifted full-bridge DC-DC converter.

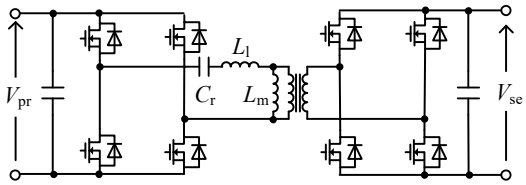


Fig. 4: LLC converter.

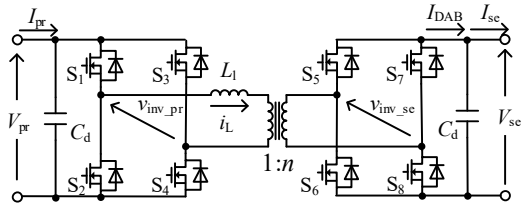


Fig. 5: Dual active bridge converter.

Table I: Characteristics of isolated DC/DC circuit topologies.

	Isolated DC/DC converter		
	Phase shift	LLC	DAB
Bidirectional operation	○	+	+
Efficiency	○	○	+
Size	−	+	+

+ : Good, − : Bad, ○ : Neutral

inductance, which avoids the downsizing of the DC-DC converter. Thus, a PSFB DC-DC converter is not suitable for isolated USPMs.

Fig. 4 shows an LLC converter. This converter has the capacitor C_r, which is connected to a transformer in series. L_l and L_m are leakage inductance and magnetizing inductance of the transformer, respectively. The LLC converter achieves soft switching by a resonance between C_r and L_l. On the other hand, the LLC converter controls the switching frequency according to the load in order to maintain the voltage transfer ratio. However, the voltage characteristic of the LLC converter is changed with the load. Then, voltage control of the LLC converter is difficult for the isolated USPM used in a wide power range. Thus, the LLC converter is also not suitable for the isolated USPM.

Fig. 5 shows a DAB converter. The DAB converter has an inductor connected to a

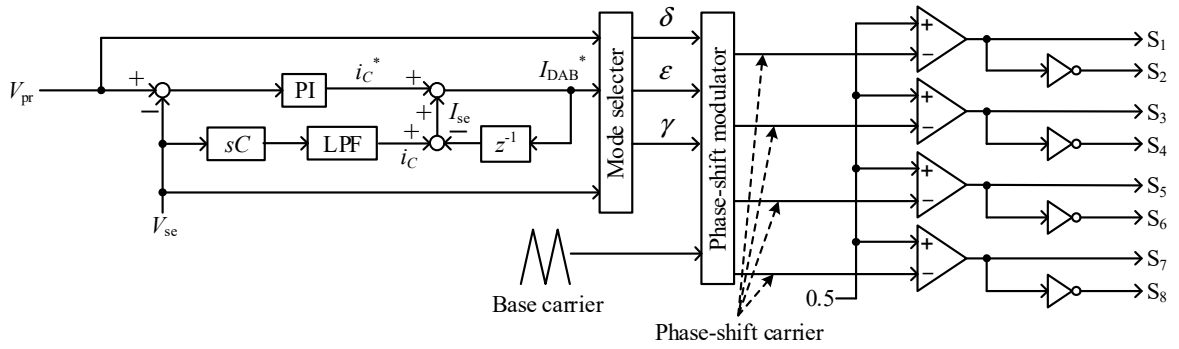


Fig. 6: Block diagram of voltage control.

transformer in series. The circuit topology is suitable for bidirectional operation because the transmission power characteristic is not changed with the power flow. In the turn ratio of the transformer matches the input-output ratio, zero voltage switching (ZVS) is achieved over the entire power range. Thus, the soft switching operation is achieved in all conditions when the isolated USPM uses the topology.

Table I lists the characteristics of the three isolated DC-DC circuit configurations. The DAB and LLC converters are suitable for bidirectional operation. The LLC converters achieve high efficiency around the rated condition, and the DAB converters have high efficiency over a wide power range [16]. Moreover, the wide-range ZVS is achieved in the DAB converter. Hence, a DAB converter is suitable for isolated USPMs.

Control strategy of isolated USPM using DAB converter

In this chapter, the key strategies are described in order to use the DAB converters as the isolated USPM.

A. Error compensation for non-linear transmission power

The transmission power of the DAB converter is controlled by the phase difference of the transformer voltage δ between the primary side and the secondary side. However, a non-linear characteristic occurs at the light load due to the dead time. The isolated UPSMs should keep linear characteristics in order to support the ideal characteristics of the UPSM-based power converters system. Thus, the effective error compensation method is adopted [17].

The error compensation method in Ref[17] controls the zero current period of the inductor current by the three-level output operation. The compensation method is divided into three modes:

1) Two-level mode for the heavy load,
2) Three-level mode I for the light load,
3) Three-level mode II for the significant light load.

The two-level mode is a two-level operation of primary and secondary inverters. Mode I operates with the zero current period fixed to the dead time by three-level operation. Mode II operates with the phase difference fixed to dead time by three-level operation.

B. Output voltage control

Fig. 6 shows a block diagram of the voltage controller for a DAB-based isolated USPM converter with the error compensation method. The command of the secondary voltage is set to the primary side voltage in order to operate as a DCX. The deviation between the primary and secondary side voltages is converted to a command current by a PI controller. The operation mode is selected depending on the command current, and the phase difference and the zero voltage periods (ε, γ) are calculated. The phase shift carrier is generated from the phase difference, the zero voltage period, and the base carrier. The voltage control has a high-speed response to disturbances by estimating the secondary side current from the secondary side voltage and the feedforward compensation. It is possible to realize a low-cost isolated USPM because the voltage control does not require a current sensor.

C. Current balance control for parallel-connected USPMs

The isolated USPMs should support parallel connections to construct high-current applications. Each USPM is an independent power converter, and each module has some

voltage detection circuits. Thus, the current imbalance among parallel-connected USPMs may occur because of detection gain errors, the line impedance imbalance, and so on. The current imbalance causes a reduction of efficiency and a breakdown of control. Therefore, the current balance must be kept. Note that current balance control must be achieved only by low-speed communication through the master controller.

Fig. 7 shows the block diagram of the current balance control, where the suffix x is the cell number of USPM, the suffix m is the number of parallel-connected USPMs, and Z is the gain of the current balance control. The current balance control calculates the imbalance current from the average value of the command current. Besides, the current balance control keeps the current balance by increasing or decreasing the voltage command value based on the imbalance current. The current balance control controls the DC current and is implemented in the outer loop of the voltage control. Therefore, the current balance control is implemented in the low-speed master controller to allow a delay in wireless communication.

The gain Z of the current balance control is designed based on the accuracy of the current balance control and its effect on the load response. Z affects the transient characteristics due to the communication delay. Therefore, it is necessary to consider not only the current balance but also transient characteristics when designing Z. The imbalance current due to the detection gain error of the secondary side voltage is obtained by

$$I_{\text{imbalance}} = \frac{V_{\text{se}}}{Z}\left(e_{\text{se\_avg}} - e_{\text{se\_}x}\right) \quad (1),$$

where $e_{\text{se\_avg}}$ is the average value of the detection gain error of the secondary side voltage, and $e_{\text{se\_}x}$ is the detection gain error of the secondary side voltage of the cell x. The maximum fluctuation of the secondary side voltage during the load step is

$$\Delta V_{\text{se\_max}} = \Delta I_{\text{DAB}} Z \quad (2),$$

where ΔI_{DAB} is the change in the secondary side current.

Z is designed by (1) and (2). The lower limit of Z is calculated from the allowable imbalance current using (1), and the upper limit of Z is calculated from the maximum allowable voltage fluctuation using (2). The current balance control achieves compensation for both current balance and voltage fluctuations during the load step by setting Z within the calculated upper and lower limits. In this paper, the allowable imbalance current is the difference between the maximum current and the rated current of the isolated USPM in order to prevent control breakdown due to the current imbalance. It is also designed so that the maximum voltage fluctuation is within 10% of the rated voltage when the secondary side current changes by 1p.u.

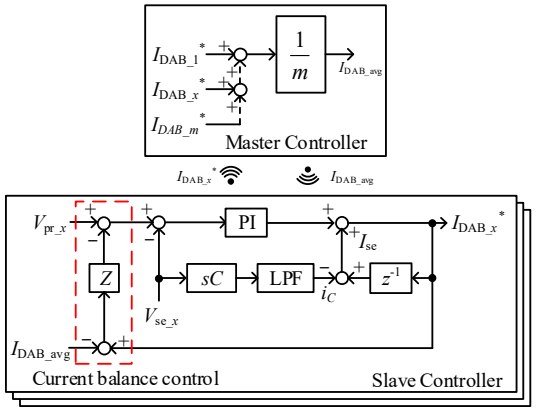


Fig. 7: Block diagram of current balance control.

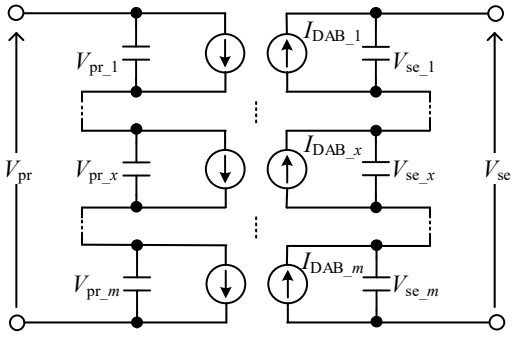


Fig. 8: Equivalent circuit of DAB converters connected in series.

D. Voltage balance control for series-connected USPMs

The Isolated USPMs should also support series connections to construct high-voltage applications. The voltage imbalance among series-connected USPMs occurs because of the gain errors of voltage detection and so on. The voltage imbalance may destroy the device.

Fig. 8 shows the equivalent circuit of the DAB converter when connected in series, where the suffix x is the cell number of the USPM, and the suffix m is the number of series-connected USPMs. The DAB converter is equivalent to a current source. Thus, the series-connected DAB converter with the independent controller is equivalent to a series-connected current source.

Then, the control interference among series-connected cells occurs. This paper applies the current droop control in order to prevent control interference.

Fig. 9 shows the block diagram of the current droop control with the voltage balance control. In addition to the current droop control, which suppresses the control interference among each USPM, the voltage balance control compensates for the voltage imbalance among series-connected USPMs. The current source interference and the voltage imbalance in the series connection of the DAB converters are changed with power flow. Hence, the current droop control switches the operation modes depending on the power flow, which is identified from the command current. However, the droop admittance Y_d of the conventional current droop control is constant. Therefore, the command value fluctuates significantly during power flow switching, which causes voltage fluctuations. The proposed control varies Y_d according to the load to achieve seamless power flow switching. Y_d is defined by

$$Y_d = \frac{I_{DAB\_avg}}{V_{se\_avg}} K_d \quad (3),$$

where K_d is the droop gain. K_d should be set to less than 1. If K_d is set to more than 1, then the operation becomes unstable because all i_{DAB} is the current id flowing in the droop admittance. The voltage balance control calculates the imbalance voltage from the average value of the secondary side voltage. It keeps the voltage balance by increasing or decreasing the voltage command value based on that value. The imbalance voltage is compensated more by increasing the gain K of the voltage balance control. Therefore, K was set to 1 in this paper. The current droop control and the voltage balance control are implemented in the outer loop of the voltage control. Therefore, the voltage balance control is implemented in the low-speed master controller to allow a delay in wireless communication.

Experimental Verification

Table II shows the experimental conditions. The dead time is set to a long time to evaluate the compensation method for the transmission power error. The effectiveness of the output voltage control during a single operation, the voltage balance control in a series connection, and the current balance control in a parallel connection are verified by the following experiments.

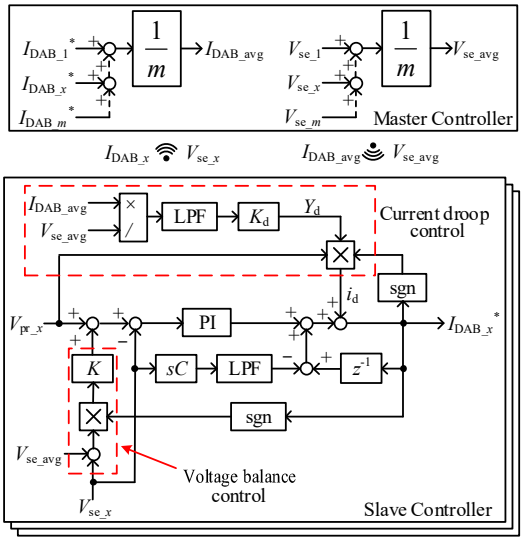


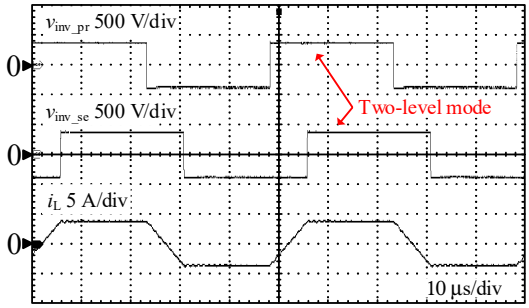
Fig. 9: Block diagram of voltage balance control.

Table II: Experimental specifications.

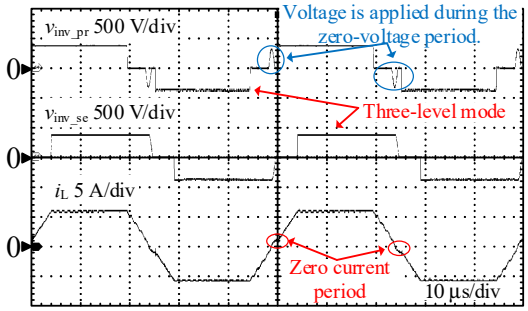
Primary side voltage	V_{pr}	380 V
Secondary side voltage	V_{se}	380 V
Rated power of one unit	P	1000 W
Leakage inductance	L_l	760 µH
Turn ratio of transformer	n	1
DC capacitance	C	60 µF
Switching frequency	f_{sw}	20 kHz
Dead time	t_{dt}	2 µs

A. One unit operation

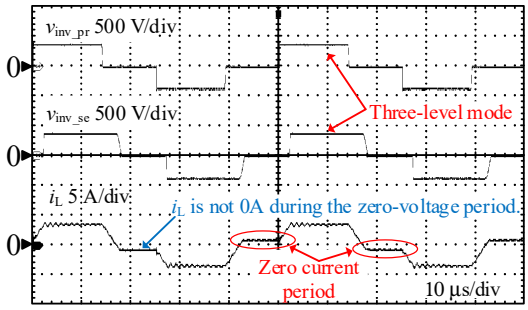
Fig. 10 shows the operating waveforms for the two-level mode and three-level mode. In this experiment, the USPM was driven by open-loop control with the voltage sources connected to the primary and secondary sides to verify each mode of operation. Fig. 10 (a) shows the operating waveform when the power command P^* = 1.0p.u. Both the primary and secondary sides are operating in two-level mode. Here, the power error to the command value is 2.7%. Fig. 10(b) shows the operating waveform when the power command P^* = 0.5p.u. The operating mode is Mode I, with the primary and secondary side voltages operating at three levels. The magnetizing inductance increases the inductor current and current flows during the zero current period. The current during the zero current period causes resonance between the leakage inductance and the parasitic capacitance of the device. Therefore, the voltage is applied during the zero voltage period of v_{inv_pr}. Furthermore, the resonance causes a power error of 26.4%.Fig. 10(c) shows the operating waveform when the power command P^* = 0.2p.u. The operating mode



(a) Two-level mode. This mode is the general operation of the DAB converter.



(b) Mode I. This mode fixes the zero current period at dead time in three-level operation.



(c) Mode II. This mode fixes the phase difference at dead time in three-level operation.

Fig. 10: Experimental waveforms of each mode.

is Mode II. In Fig.10(c), the inductor current i_L during the zero current period has a slight current flow. This reason is a delay in the discharge from the parasitic capacitance due to hard switching on the secondary side, which delays the start of the zero current period. The power error of 36.4% occurs due to the delay in the start of the zero current period. The cause of these errors is the magnetizing inductance, and therefore the transformer must be redesigned.

Fig. 11 shows the transmission power characteristics. The characteristics without error compensation are non-linear at light loads, but the

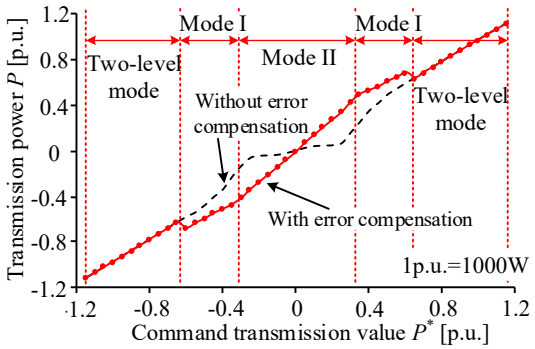


Fig. 11: Characteristic of transmission power in single DAB unit operation.

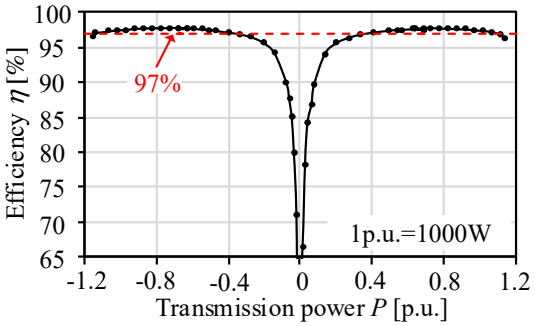
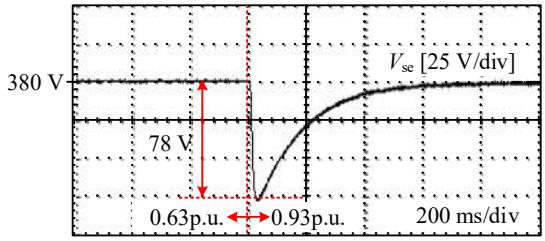


Fig. 12: Efficiency characteristic of a DAB converter.

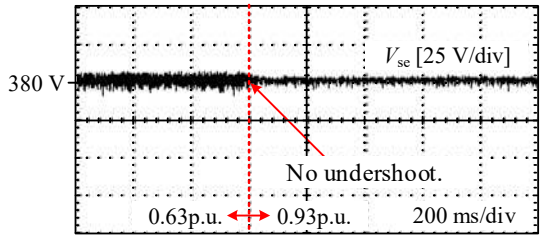
characteristics with the error compensation method are nearly linear. On the other hand, the transmission power is higher than the commanded value during three-level operation. This is caused by the voltage applied during the zero voltage period in Fig. 10(b) and the current flowing during the zero current period in Fig. 10(c).

Fig. 12 shows the efficiency characteristics of the DAB converter. The efficiency exceeds 97% at 0.4p.u. or higher, enabling high-efficiency operation over a wide bidirectional power range. These results verify the effectiveness of the DAB converter as the main circuit scheme for the isolated USPMs, which require high-efficiency operation over a wide power range.

Fig. 13 shows the operating waveforms when the load is changed stepwise from 0.63p.u. to 0.93p.u. in the voltage control of Fig. 6. Fig. 13(a) shows the waveform when the estimated Ise is not compensated feedforward. The secondary side voltage fluctuates by 78V during the load step. Fig. 13(a) shows the waveform when the estimated I_{se} is compensated feedforward. The secondary side voltage does not fluctuate during the load step. Thus, the control of Fig. 6 achieves a high response to disturbances without a current sensor.



(a) Without feedforward compensation of estimated I_{se}.



(b) With feedforward compensation of estimated I_{se}.

Fig. 13: Experimental waveform of load step in single DAB unit operation.

B. Parallel connection

Two DAB converters are connected in parallel to verify the effectiveness of the current balance control. These DAB converters are driven by two independent controllers, respectively. In addition, a detection gain error of 1% is added to the secondary side voltage of the DAB converter at cell #1. Note that the effect of the detection gain error is almost the same as the impedance imbalance of the connecting wire for each USPM. Moreover, the circulating currents due to asynchronous carriers occur. In this experiment, an LC filter with a cutoff frequency of 2 kHz is connected to suppress the circulating current. In the future, the suppression method of the circulating current without additional components must be needed to achieve compact USPMs.

Fig. 14 shows the experimental waveforms without the current balance control at a parallel connection. In this experiment, the load is varied from 1.31p.u. to 1.97p.u. The current imbalance rate before the load change is 77.9%, and after the change is 16.8%. Note that the current imbalance rate α_I is defined by

$$\alpha_I = \frac{I_{se\_1} - I_{se\_avg}}{I_{se\_avg}} \quad (4),$$

where I_{se_avg} is the average of I_{se_1} and I_{se_2}. The current imbalance rate increases at light loads.

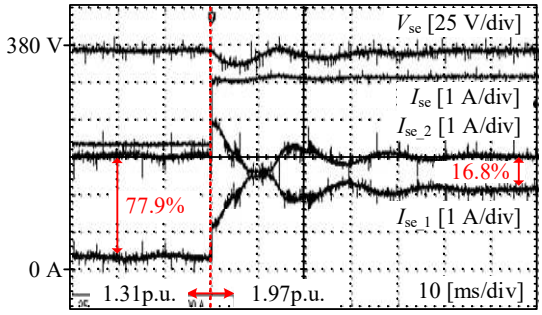


Fig. 14: Experimental waveforms of load step in parallel connection without the current balance control.

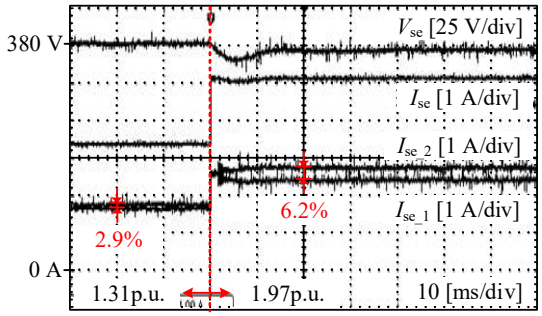


Fig. 15: Experimental waveforms of load step in parallel connection with the current balance control.

This is because the secondary side current of the DAB converter at cell # 2 did not change before and after the load step. The phase difference of the DAB converter at cell # 2 at tt time is fixed at 90 degrees and is not improved by the voltage control interference. Therefore, only the DAB converter at cell # 1 changes the current, and the current imbalance increases at light loads.

Fig. 15 shows the experimental waveforms with the current balance control at a parallel connection. The allowable imbalance current is 0.25A, and the allowable voltage fluctuation is 38V in this experiment. From (1) and (2), the lower and upper limits of Z are 7.6 and 14., respectively. Therefore, Z is set to 10. In this experiment, the load is varied from 1.31p.u. to 1.97p.u. The current imbalance rate before the load change is 2.9%, and after the change is 6.2%. The current balance control improves the current imbalance rate by 75.0pt. at 1.31p.u. and by 10.6pt. at 1.97p.u. The imbalance current is 0.05 A before the load step and 0.16 A after the load step, which is less than the allowable imbalance current. Thus, the imbalance of the secondary side current due to the detection gain error is compensated by the current balance control.

C. Series connection

Two DAB converters are connected in series to verify the effectiveness of the voltage balance control. The primary side voltage is set to 380 V. These DAB converters are driven by two independent controllers, respectively. In addition, a detection gain error of 1% is added to the secondary side voltage of the DAB converter at cell #1.

Fig. 16 shows the experimental waveforms without the voltage balance control at the series connection. In this experiment, the load is varied from 0.36p.u. to 0.49p.u. The voltage imbalance rate before the load step is 37.5%, and the imbalance rate after the load step is 16.1%. Note that the current imbalance rate α_V is defined by

$$\alpha_{V\_se} = \frac{V_{se\_1} - V_{se\_avg}}{V_{se\_avg}} \quad (5),$$

where V_{se_avg} is the average of V_{se_1} and V_{se_2}. The imbalance rate increases at light loads. In addition, the phase difference of the DAB converter at cell # 2 at this time is fixed at 90 degrees and is not improved by the voltage control interference.

Fig. 17 shows the experimental waveforms with the voltage balance control at the series connection. The droop gain K_d of the voltage droop control is set to 0.7, and the gain K of the voltage balance control is set to 1. The load is varied from 0.36p.u. to 0.49p.u. The voltage imbalance rate before the load step is 0.5%, and the imbalance rate after the load step is 1.0%. The voltage balance control improves the voltage imbalance rate by 37.0pt. at 0.36p.u. and by 15.1pt. at 0.49p.u. The imbalance of the voltage caused by detection gain errors is compensated by the voltage balance control.

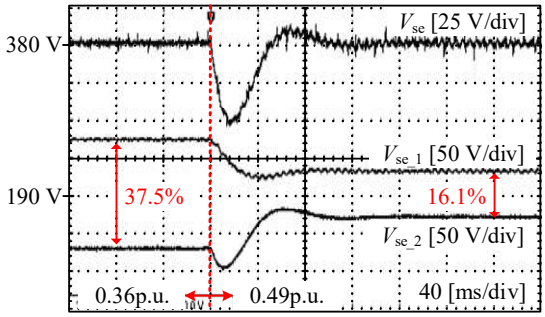


Fig. 16: Experimental waveforms of load step in series connection without the voltage balance control.

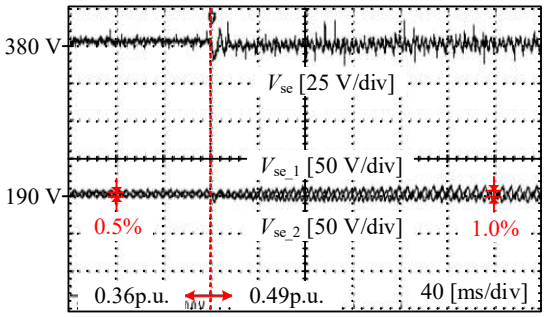


Fig. 17: Experimental waveforms of load step in series connection with the voltage balance control.

Conclusion

In this paper, the circuit topology and control for an isolated USPM were investigated. The DAB converter was selected as the circuit configuration because of its suitable bidirectional performance and high efficiency. The experimental verification with a single unit verified that the efficiency exceeds 97% at 0.4p.u. or higher and that high-efficiency operation was possible over a wide power range. The current and voltage balance control methods for the isolated USPMs in parallel and series connections were verified by the experiment. As a result, the current imbalance rate at 1.31p.u. was improved by 75.0pt. in parallel connection, and the voltage imbalance rate at 0.36p.u. was improved by 37.0pt. in series connection. In the future, we plan to verify power balance control that combines voltage balance control and current balance control in a series-parallel connection.

References

[1]. B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D.P. Kothari: A Review of Single-Phase Improved Power Quality AC–DC Converters, IEEE Transactions on Industrial Electronics, Vol. 50, No. 5 pp.962-981, 2003.

[2]. J. Xu, C. Zhao, Y. Xiong, C. Li and T. An: Optimal Design of MMC Levels for Electromagnetic Transient Studies of MMC-HVDC, IEEE Transactions on Power Delivery, Vol. 31, No. 4 pp.1663-1672, 2016.

[3]. T. Qandari and B Tousi: Single-Source Three-Phase Multilevel Inverter Assembled by Three-Phase Two-Level Inverter and Two Single-Phase Cascaded H-Bridge Inverters, IEEE Transactions on Power Electronics, Vol.36, No.5 pp.5204-5212, 2021.

[4]. M. Ma, X. He, R. Zhao and D. Wang: Synchronization Analysis of Space-Vector

PWM Converters With Distributed Control, IEEE Transactions on Power Electronics, Vol. 25, No. 12, pp.3026-3036, 2010.

[5]. A. R. Iyer, R. Moghe, R. Kandula, J. Hernandez and D. Divan: Validation of the Plug-and-Play AC/AC Power Electronics Building Block (AC-PEBB) for Medium-Voltage Grid Control Applications, IEEE Transactions on Industry Applications, Vol. 50, No. 5, pp.3549-3557, 2014.

[6]. Á. Mayor, M. Rizo, A. R. Monter and E. J. Bueno: Commutation Behavior Analysis of a Dual 3L-ANPC-VSC Phase-Leg PEBB Using 4.5-kV and 1.5kA HV-IGBT Modules, IEEE Transactions on Power Electronics, Vol. 34, No. 2, pp.1125-1141, 2018.

[7]. K. Yamanokuchi, H. Watanabe and J. Itoh: Droop-based Current Control Method in Autonomous Distributed Modula Power Conversion System, APEC 2021, pp.660-667.

[8]. M. Sakamoto and H. Haga: Control Method for Universal Smart Power Module Considering Wireless Communication, IEEJ Journal of Industry Applications, Vol. 12, No.2, pp.204-214,2023.

[9]. D. Hiroe, X. Zhang, K. Nakamura, K. Sato, R. Suzuki, K. Yoshimoto and T. Yokoyama: A Study of 10MHz Multi-Sampling Deadbeat Control for PMSM Drive System using USPM Controller, IEEJ Journal of Industry Applications, Vol. 12, No. 3, pp. 508-516

[10]. S. Iyasu, Y. Hayashi, Y. Handa, K. Nakamura and K. Wada: Suppression for DC Magnetic Flux for a Current-Fed Bi-Directional Isolated DC-DC Converter under Boost Mode, IEEJ Transactions on Industry Applications, Vol. 140, No.9, pp. 673-684, 2020.

[11]. S. Kim, H. Cha, H. F. Ahmed, B. Choi and H. Kim: Isolated Double Step-Down DC–DC Converter With Improved ZVS Range and No Transformer Saturation Problem, IEEE Transactions on Power Electronics, Vol. 32, No. 3, pp. 1792-1804, 2017.

[12]. T. Jiang, J. Zhang, X. Wu, K. Sheng and Y. Wamg: A Bidirectional LLC Resonant Converter With Automatic Forward and Backward Mode Transition, IEEE Transactions on Power Electronics, Vol. 30, No. 2 , pp.757-770, 2015.

[13]. H. Li, S. Wang, Z. Zhang, J. Zhang, M. Li, Z. Gu, X. Ren and Q. Chen: Bidirectional Synchronous Rectification ON-Line Calculation Control for High Voltage Applications in SiC Bidirectional LLC Portable Chargers, IEEE Transactions on Power Electronics, Vol. 36, No. 5, pp.5557-5568, 2020.

[14]. S. Inoue and H. Akagi: Operating Voltage and Loss Analysis of a Bi-Directional Isolated DC/DC Converter, IEEJ Transactions on Industry Application, Vol. 127, No.2, pp. 189-197, 2007.

[15]. N. Hou, L. Ding, P. Gunawardena, Y. Zhang and Y. W. Li: A Comprehensive Comparison of Two Fast-Dynamic Control Structures for the DAB DC–DC Converter, IEEE Transactions on Power Electronics, Vol.37, No. 6, pp.6488-6500, 2021.

[16]. R. Yamada, A. Hino and K. Wada: Improvement of Efficiency in Bidirectional DC-DC Converter with Dual Active Bridge Using GaN-HEMT, IEEJ Journal of Industry Applications, Vol. 12, No. 3, pp. 254-272, 2023.

[17]. K. Kawauchi, H. Higa, H. Watanabe, K. Kusaka and J. Itoh: Current Reduction Method for Dual Active Bridge Converter in Non-liner Dead-time Compensation Method, IEEJ Transactions on Industry Applications, Vol.140, No. 3, pp.175-183,2020.