Signal Wireless Carrier Synchronization Using Power Line for Interleaving in Power Converters

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***Abstract*— This paper proposes a carrier synchronization method that does not require synchronous signal lines and a time synchronization module, such as a GNSS module. For interleaved and multilevel operations, all carriers must be synchronized in order to align the switching timing. In a distributed control system with multiple controllers, signal lines or additional time modules are required for synchronization, reducing maintainability and cost. In this paper, the proposed carrier synchronization is performed by superimposing a synchronization signal on the power line. The proposed control method is demonstrated by simulation, showing that the synchronization accuracy is within 0.2 μs. Especially this method is effective in realizing electrified systems in severe conditions, such as in the sectors of construction machinery, aircraft, and aerospace.**

Keywords*— carrier synchronization, interleaving, multilevel, modular multilevel converter, distributed control, electrification, construction machinery

I. INTRODUCTION

Power converters are required to be compact and high-power density. Increasing equivalent switching frequency by interleaving or multilevel operation is a popular technique to expand the operation range of the power converter [1]-[4]. Interleaving and multilevel operations require synchronized carriers. Thus, one of the following system configurations must be adopted; 1) a single controller manages all cells, and 2) signal wires among controllers are added to share the synchronization signal with a few microseconds of accuracy. Some of the carrier synchronization methods with signal lines are based on controller area network (CAN), EtherCAT, and a customized protocol based on Ethernet [5]-[7]. The disadvantage of these methods is that the signal wires and additional components for synchronization are needed. These components bring increasing costs and limited reliability.

In contrast, power line communication (PLC) has attracted in some industrial fields such as the Internet of Things (IoT) devices and factory automation to reduce signal wires [8]-[9]. The PLC technique superimposes high-frequency signals on power lines at the transmitter and uses the power lines as transmission lines. After arriving at the receiver, the data is recovered by separating the high-frequency components of the power line. The future of PLC is promising with the publication of IEEE Std. 1901-2020 as a standard specification for physical (PHY) and medium access control (MAC) layers [10]. The advantage of PLC is communicable without signal lines. Meanwhile, PLC needs additional circuits and signal wires for the superimposing and extraction.

[11]-[13] proposed superimposing data signals to the power line by changing the switching frequency without additional circuits for PLC. These proposals will greatly expand the PLC application because data transmission and power conversion are integrated. However, these studies focused on data communications, and carrier synchronization using PLCs is not assumed. The carrier synchronization using the power line requires high-precision synchronization with low jitter compared to data transmission. Thus, carrier synchronization using a power line is a challenging approach.

Meanwhile, as another approach, a carrier synchronization technique has been proposed using the high-precision synchronization signal utilizing global navigation satellite system (GNSS) signals [14]. In [14], a synchronized trigger is obtained by pulse per signal (PPS), which has high synchronization accuracy and enables wireless carrier synchronization among independent controllers within ±80 ns synchronization error. The method reduces signal wires among independent controllers for synchronization. However, GNSS brings two disadvantages; 1) GNSS cannot be used in radio-shielded spaces, 2) Increasing costs by GNSS modules.

This paper proposes a carrier synchronization method that does not require synchronous signal lines and a time synchronization module, such as a GNSS module. The proposed method has three steps; 1) the carrier synchronous reference signal is generated in the low-frequency region where it is easy to detect, 2) the carrier synchronous reference signal is extracted by each controller, 3) Frequency multiplying reference signal to carrier frequency. This allows the controllers to generate high-precision carrier synchronous signals without additional components. Thus enabling the controller to be signal wireless while preventing high controller costs.

The new contributions of the proposed method are that 1) synchronization at the carrier level is achieved without signal wires and additional time synchronization components, such as GNSS module, 2) the synchronization is continuously achieved in radio-shielded placements such as in basements, reinforced-concrete buildings, and metal frames. The

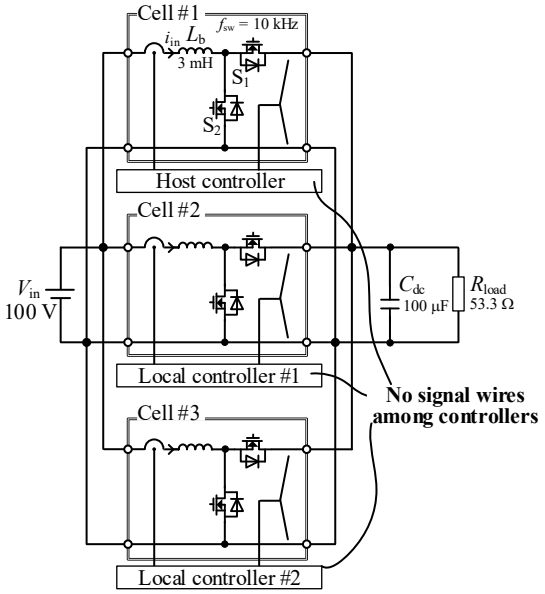


Fig. 1. Main circuit. A boost converter is used. The proposed carrier synchronization method is also acceptable to various circuit topologies, such as a dual active bridge (DAB) converter or a phase shift full bridge (PSFB) converter. There are no signal lines among controllers. The carrier synchronization is performed based on the signal, which are superimposed on the output voltage detected by each controller.

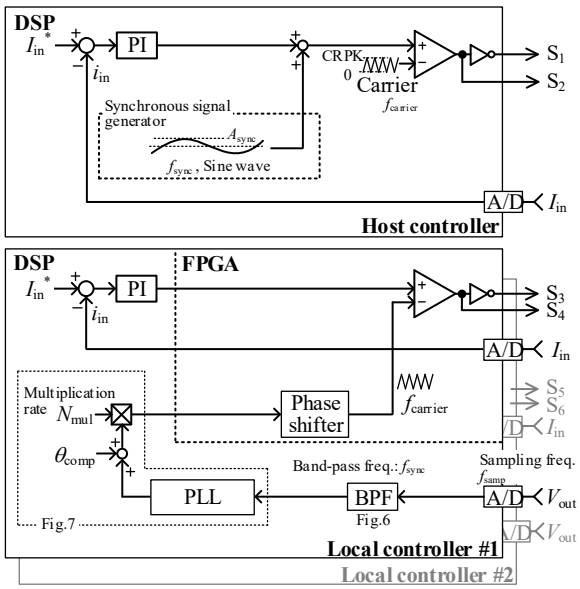


Fig. 2. Proposed control system.

proposed method is simulated by three boost converter with each independent controller. From the simulation results, the synchronization accuracy within 0.5 μs is achieved. Furthermore, the characteristics of the proposed method are partially verified by fundamental experiments.

II. System Configuration

A. Main Circuit

Fig. 1 shows the targeted circuit in this study. Three boost converters are connected in parallel. A DC power supply is connected to the input, and a resistive load is connected. Each converter is driven by an independent controller, and the controller clocks are not synchronized among controllers.

B. Controller

Fig. 2 shows the controller configuration. One controller is attached to each converter, for a total of three controllers. One of the controllers is the host controller, and the others are local controllers. The local controllers are controlled to synchronize with the host controller's carrier based on the synchronization signal from the host controller. The host controller consists of a digital signal processor (DSP) with a current proportional-integral (PI) controller and a carrier synchronous signal generator. The local controller consists of a DSP and a field programmable gate array (FPGA). The function of DSP are a bandpass filter (BPF) that extracts the carrier synchronous signal, a phase-locked loop that multiplies from the reference signal to the carrier frequency. The functions of FPGA are as a phase shifter to achieve the interleaving and a comparator to implement carrier-based modulation.

III. Principle of Proposed Carrier Synchronous Method

Fig. 3 shows the outline of the proposed wireless carrier synchronization method. The proposed method consists of the following three steps.

A. Superimposing carrier synchronous signal

The carrier synchronous signal $u_{\mathrm{sync}}(t)$ is expressed as

$$u_{sync}(t) = A_{sync} \sin(2\pi f_{sync} t) \quad (1),$$

where A_{sync} is the amplitude of the synchronous signal, and f_{sync} is the frequency of the synchronous signal. The synchronous signal $f_{\mathrm{sync}}(t)$ is superimposed on the output of the input current PI controller. The zero degree of the carrier synchronous signal is aligned on the bottom of the carrier.

B. Extracting component of carrier synchronous signal using BPF

The synchronous signal frequency component is detected by the local controller using a BPF. The bandpass frequency is matched to the synchronous signal frequency f_{sync} to extract the synchronous signal component in the output voltage. In designing the BPF, the phase characteristics should be linear and gradual near the synchronous signal frequency. The reason is to easily compensate the phase lead or lag due to the BPF.

C. Reference signal restoration and frequency multiplying

The phase of the reference carrier is obtained by a PLL with a frequency multiplier at the local controller based on the BPF output. Then, the feed-forward compensation of phase delay is needed. The estimated delay of recovered synchronous signal T_{rcvy} is given by

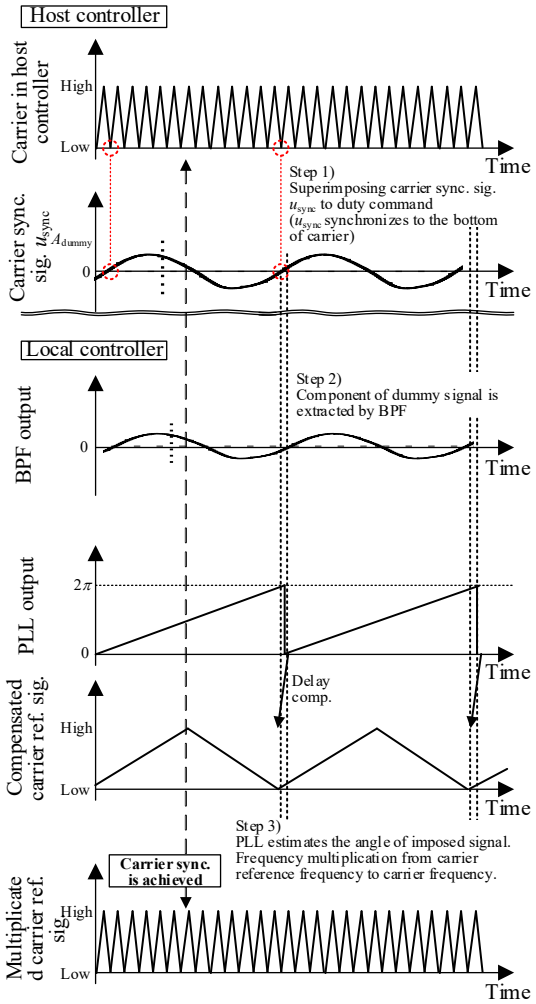


Fig. 3 Outline of proposed carrier synchronization using power line.

TABLE I. CIRCUIT PARAMETERS.

Name	Symbol	Value
Input voltage	V_{in}	100 V
Number of cells	N	3
Rated output power	P	1 kW
Boost inductor	L_b	3 mH
Load resistance	R_{load}	53.3 Ω
Output capacitance	C_{out}	100 μF (H = 2.67 ms)

H: Unit capacitance constant

TABLE II. CONTROLLER PARAMETERS.

Parameter	Symbol	Value
Sampling frequency	f_{samp}	100 kHz
Carrier frequency	$f_{carrier}$	10 kHz 20 kHz (in Chap. V)
Controller bandwidth for input current	ω_{PIi} f_i	2000 rad/s 318.3 Hz
Amplitude of carrier sync. sig.	A_{sync}	12 V (±10 % duty variation)
Frequency of carrier sync. sig.	f_{sync}	625 Hz 1250 Hz (in Chap. V)
Multiplication rate	N_{mul}	16 8 (in Chap. V)

$$T_{rcvy} = T_{v-i} + T_{det} + T_{ADC} + T_{BPF} + T_{PLL} \quad (2),$$

where $T_{v\text{-}i}$ is the phase delay of output voltage from the carrier synchronous signal. The phase delay $T_{v\text{-}i}$ is

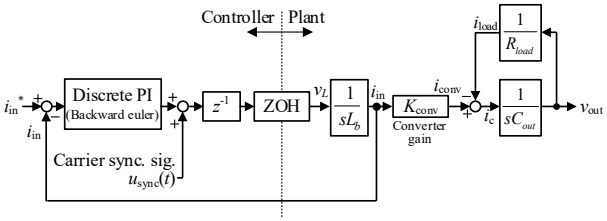


Fig. 4 block diagram of input current controller and load.

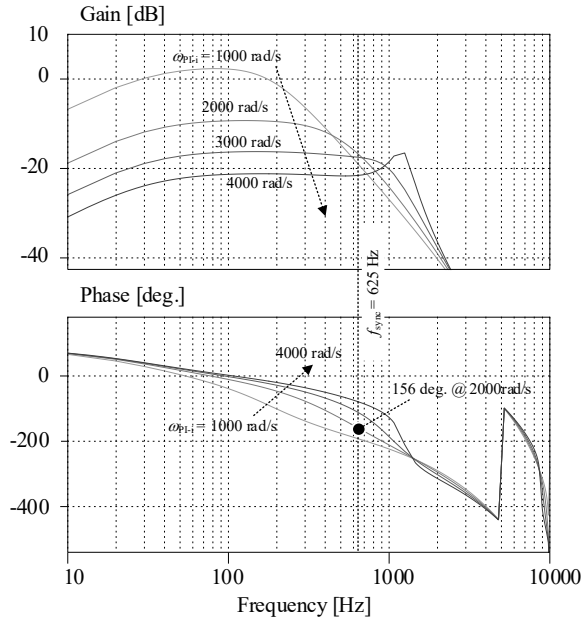


Fig. 5 Frequency characteristic of output voltage from carrier synchronous signal v_{out}/u_{sync}.

determined by the controller bandwidth, the output capacitance, and the load resistance. T_{det} is the delay at the detection circuit, T_{ADC} is the delay at the AD converter, T_{BPF} is the phase delay at the BPF, T_{PLL} is the delay at the PLL.

In this paper, delays due to T_{det}, T_{ADC}, T_{BPF}, and T_{PLL} are assumed to be zero and are not included in the simulation model. The assumption is based on two reasons; 1) constant delay (i.e., easy compensation), 2) These delay are not dominant for $T_{v\text{-}i}$.

Hence, this paper focuses on the dominant phase delay in recovered synchronous signal T_{rcvy} which is composed only $T_{v\text{-}i}$. From these assumptions, (2) is approximated by

$$T_{rcvy} \approx T_{v-i} \quad (3).$$

IV. CONTROLLER DESIGN

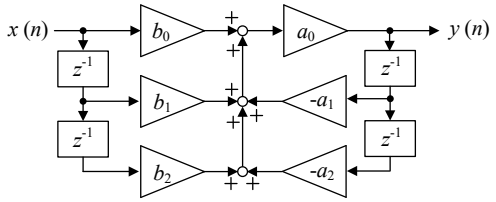
Table I lists the circuit parameters. The input is connected to 100V DC. A resistive load and a output capacitor is connected at output terminals of boost converters. Table II lists the controller parameters.

A. Input current controller

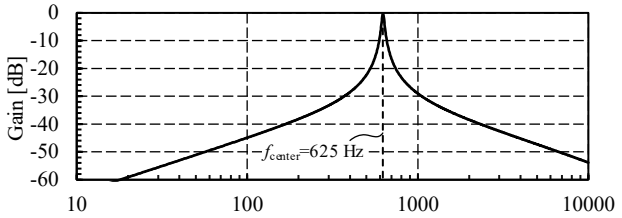
The host controller superimposes the carrier synchronous signal u_{sync} on the output of the current PI controller. Hence, the carrier synchronous signal is as a disturbance to the

TABLE III. DESIGN PARAMETERS FOR BAND-PASS FILTER

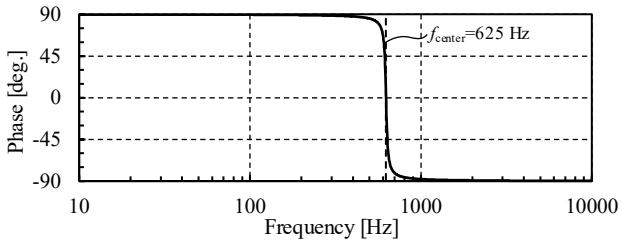
Parameter	Symbol	Value
Sampling frequency	f_{samp}	100 kHz
Center frequency	f_{center}	625 Hz
Band-pass width	BW	0.05 octave
Coefficients	a_0	1.0007
	a_1	-1.9985
	a_2	0.9993
	b_0	0.0007
	b_1	0.0000
	b_2	-0.0007



(a) block diagram.



(b) Gain characteristic.



(c) Phase characteristic.

Fig. 6. Implementation of bandpass filter.

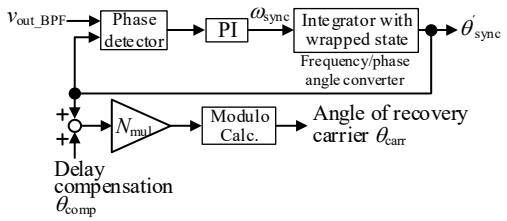


Fig. 7 Implementation of PLL and frequency multiplier.

current PI controller. The control bandwidth of input current PI controller must be limited in order to prevent a elimination of the synchronous signal.

Fig. 5 shows the frequency characteristic of output voltage from carrier synchronous signal v_{out}/u_{sync}. In the proposed method, the synchronous signal frequency is set to around a few hundred Hz to a few kHz. The component of the synchronous signal is eliminated due to increasing the control bandwidth. The control bandwidth is set to 2000 rad/s to prevent the elimination of the imposing signal. Moreover, the bandwidth of the input current controller at local controllers should be set to the same value. When designed for 2000 rad/s, the output voltage phase is -156deg compared with the synchronous signal.

B. Band-pass filter

Table III lists the coefficients of the infinite impulse response(IIR) filter. The second-order IIR filter is employed as the BPF. Fig. 6 shows the frequency characteristics of the BPF. The transfer function of the IIR filter is expressed as

$$G_{IIR}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \quad (4),$$

where a_k and b_k are filter coefficients. The transfer function of typical BPF is given by

$$G_{BPF}(s) = \frac{\frac{\omega_{center} s}{Q}}{s^2 + \frac{\omega_{center}}{Q} s + \omega^2_{center}} \quad (5),$$

where ω_{center} is $2\pi f_{center}$ and Q is quality factor. Here, the filter coefficients a_k and b_k are obtained by transforming (5) into the z-domain using the bi-linear transformation.

C. PLL and frequency multiplier

Fig. 7 shows the implemented PLL and frequency multiplier. This study employs an enhanced PLL. The phase detector involves an adaptive notch filter to improve the tracking performance of PLL. The PLL output synchronizes with the synchronous signal u_{sync} by the host controller. The multiplication rate is determined by

$$N_{mul} = \frac{f_{carrier}}{f_{sync}} \quad (6).$$

For simplicity of implementation, the multiplication rate should be set to a power of 2. In this paper, carrier frequency $f_{carrier}$ and carrier synchronous signal frequency f_{sync} are set to 10 kHz and 625 Hz, respectively. Thus, the multiplication rate N_{mul} is set to 16, respectively. The delay compensation θ_{comp} is set to

$$\theta_{comp} = 2\pi \frac{T_{rcvy}}{T_{sync}} \quad (7).$$

V. SIMULATION RESULTS

Fig. 8 shows the simulation result with the proposed carrier synchronization method. By superimposing a 1.25 kHz carrier synchronous signal u_{sync} on the duty command, the frequency component of the signal frequency is involved the output voltage with the phase delay δv-i. By correcting the delay and the delay of the BPF filter, the synchronous signal is recovered. By multiplying the PLL output with the multiplication rate N_{mul}, the carrier of the local controllers are synchronized with the carrier of the host controller. From the simulation results, the synchronization accuracy within -0.21 μs (-0.72 deg) is achieved. Hence, the proposed method has

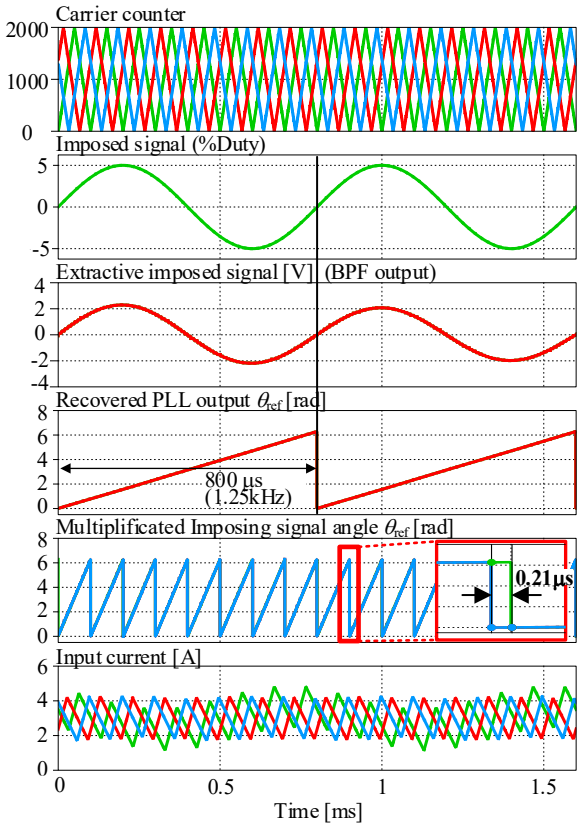


Fig. 8 Simulation result (f_{sync} = 1.25 kHz, f_{sw} = 20 kHz).

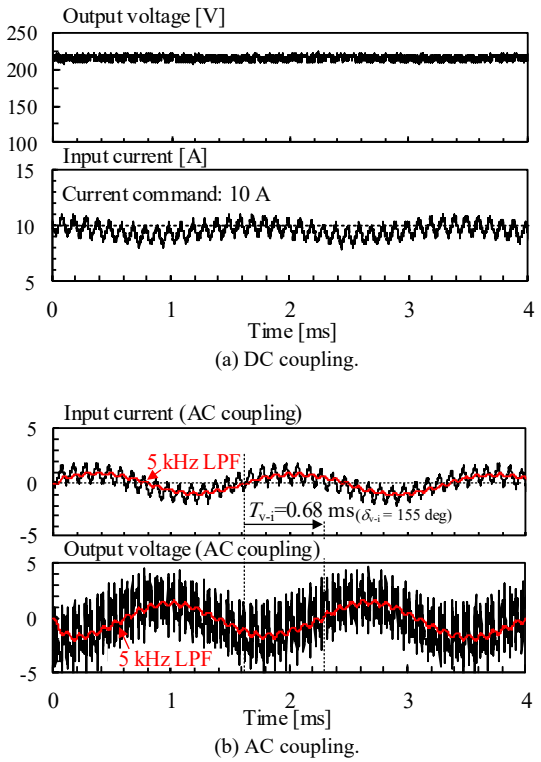


Fig. 9. Experimental waveforms of input current and output voltage at rated output (1 kW) when the host controller only operates. The synchronous signals were generated by varying duty cycle by ±10%.

the potential to achieve interleaving without wired communication.

VI. Fundamental Experiment

Fig. 9 shows the input voltage and the input current at the rated output when cell #1 only operates. The input voltage and the input current are measured with AC coupling mode in Fig. 9 (b). The phase difference between input current and output voltage $\delta_{v\text{-}i}$ is -155 deg. This is the phase difference determined by the control bandwidth of the input current controller, the output capacitor, and the load. Meanwhile, the analysis in Figure 5 shows a delay of -156 deg. Therefore, the theoretical model (Fig. 4) agrees with experimental results.

VII. Conclusion

This paper proposed a carrier synchronization method without signal lines that realize interleaving using a power line. In the proposed method, a low-frequency carrier synchronous signal is superimposed on the power line, and each controller detects the signal individually. The signal multiplys to the switching frequency.

The proposed method generates the carriers with high accuracy while reducing the sampling frequency required for the controller. Thus, the proposed method has two features; 1) no restrictions on the location of use, 2) no additonal components for the carrier synchrnonization. From the simulation results, the synchronization accuracy within -0.21 µs (-0.72 deg) is achieved.

In future work, the experimental verification will be scheduled. In addtion, the relationship between transient carrier synchronization accuracy during load fluctuations will be studied.

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