Distributed Control Method for Power Conversion System With Series-Connected Autonomous Modular Converters

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***Abstract*—This article proposes a current droop control for series-connected current source converters in a universal smart power module (USPM) concept. In this concept, power conversion systems are constructed by USPMs, which have a high-speed controller and autonomous distributed control. USPM enhances versatility by its high flexibility and usability compared to power electronics building blocks, which is a similar concept. In this system, noninterference control is required because these USPMs are operated independently without sharing information with each other. Droop control for the voltage source converter is a common solution for parallel-connected converters. Likewise, a stabilization method for the current-source-type converter connected in series is necessary for the USPM system. The proposed method in this article solves these problems. In particular, the configuration of the current controller and its gain design method is verified in order to achieve a stable condition and high-speed response. The experimental results for the 500-W system reveal that the stability limit of the PI control adopting the proposed current droop control agrees with the analytical results with an error of 1.3%. Furthermore, this article demonstrates that the current deviation agrees with that of the design value with an error of 3.0% or less.**

***Index Terms*—Distributed control, power conversion, power electronics building block (PEBB), stability analysis, universal smart power module (USPM).**

I. Introduction

IN RECENT years, the low-carbon solution and energy conservation have become important missions for the realization of a sustainable society. One of the main applications in power electronics systems is renewable energy sources, such as photovoltaic, wind turbine, and energy storage systems. These power electronics systems require various types of power converters that have different specifications, which correspond to various operating requirements. At present, power electronics design requires several forms of complex and multifaceted knowledge, e.g., electronics design, thermal design, electromagnetic interference (EMI), and control.

Modular power converter systems represented by power electronics building blocks (PEBBs) have been developed in order to simplify power electronics design [1], [2], [3]. The concept of the PEBB is that the voltage and current ranges are changed by stacking power converters that perform specific power conversions for quick system buildup. Thus, the PEBB has high productivity in the main power circuit in terms of lower development cost, reduced lead time, and increased product lineup. However, the PEBB is not designed as a module to realize all kinds of power converters. The PEBB is designed for specific converter systems as well as conventional power converters. In addition, the controller, EMI filter, and other passive components are not modularized. Therefore, the power conversion system with the PEBB must be designed specifically for the application. Therefore, the PEBBs remain a challenge for general-purpose use and quick system design [4], [5], [6]. McGrath et al. [7] and Mathe et al. [8] realized further simplification of the main circuit design by a modular structure that includes a microcontroller and a detection circuit. However, their modules are not flexible enough to be adopted by other power conversion systems and applications because the module structure and microcomputer are designed specifically for the required application. In addition, the input/output filters for connecting to other equipment have to be redesigned every time the system specifications are changed [4]. For these reasons, PEBBs are not sufficient in terms of building blocks for power converters.

The authors have proposed a new modular concept, universal smart power module (USPM) concept, to achieve higher versatility systems [9]. USPM is a power module that has all power electronics elements of a main circuit, a high-speed controller, a gate driver, and an EMI filter. The essential difference between USPM and PEBB is that the USPM realizes an ideal voltage-source or current-source power supply, including filters and high-speed controllers inside the module, whereas the PEBB realizes a component of the main circuit. Thus, the USPM does not need to consider complex internal structures and controls in order to construct the power conversion system. This means that USPM systems can be designed quickly by

Manuscript received 3 February 2023; revised 8 May 2023; accepted 2 August 2023. Date of publication 23 August 2023; date of current version 23 October 2023. This work was supported by the Council for Science, Technology and Innovation, Cross-Ministerial Strategic Innovation Promotion Program, "Energy Systems of an Internet of Energy (IoE) Society" (Funding agency: JST). Recommended for publication by Associate Editor J. Liu. *(Corresponding author: Koki Yamanokuchi.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3304417.

Digital Object Identifier 10.1109/TPEL.2023.3304417

just combining USPMs. In addition, USPM reduces the failure cost of modules, because USPM only requires the same module, whereas PEBB requires different types of modules for different systems or different conversions within a system. A master controller should control multiple USPMs at the same time in order to construct the power conversion system. However, the master controller monitors the input/output information of the USPM and simply gives the voltage and current commands to each USPM. The USPM system has extreme versatility because various power electronics systems are constructed by only changing the combination of USPMs. This versatility is expected to increase the number of system designers because it allows various power conversion systems to be designed quickly and easily anywhere. This means that the USPM system can make a significant contribution to modern society, which requires the development of a wide variety of power conversion systems.

However, each USPM control interferes with other USPM controls due to an unbalance of the physical parameters, resulting in power unbalance and instability when USPMs are connected in multiple series and parallel. The autonomous distributed control for the voltage source converters connected in parallel has been widely considered as a way to solve this problem [10], [11], [12]. In particular, the droop control of voltage, frequency, and active and reactive powers has been adopted for the parallel operation of the voltage-sourced power converters in microgrids and other applications [13], [14], [15]. Current droop control can perform its task whatever the reliability of the wireless communication because high-speed communication does not have to be used. On the other hand, the series drive of current-source power converters has not been considered because, previously, there have been no applications. In addition, the current droop control requires new design guidelines without standards, whereas the voltage droop control has standards for the voltage derating of the dc bus voltage.

This article proposes the current droop control for series-connected current source converters in the USPM system. The proposed method is realized by using the duality with the voltage droop control in the master controller. The innovative aspect of this article is the proposed concept of USPM, which is a very versatile module unmatched by conventional power converters. The analysis and design of the current droop control are also the second new contribution in this article. In addition, the third new contribution is that droop gain is designed to focus on the low-frequency characteristics of the current droop control. The experimental results demonstrate the validity of the analytical results in a 1-kW single-phase system with two current source modules connected in series.

II. USPM Concept

Fig. 1 shows the system configuration of USPM and PEBB. The basic idea of the PEBB concept is that the power modules are stacked depending on the requirement of the voltage and current rating in larger scale power conversion systems, as compared to one power module. The PEBB concept is expected to improve productivity due to the shortening of the cost reduction and development period because the development of the main circuit is limited to only each module. In addition, PEBBs have

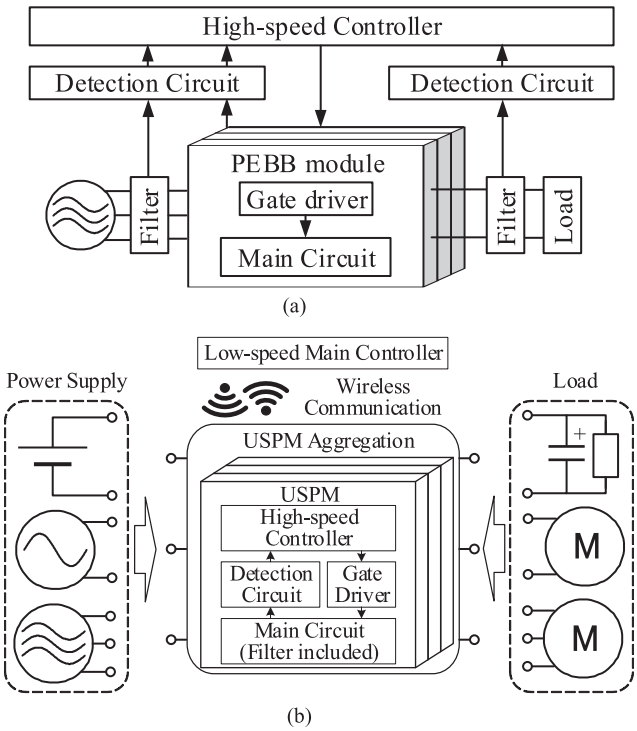

Fig. 1. Power conversion system based on the USPM concept. A high-speed controller is included in USPM compared to the conventional modular system. Various applications are adopted by transmitting a command to USPM through wireless communication. (a) PEBB. (b) USPM.

high maintainability, which can be repaired by replacing only the defective board, and high reliability, which can continue operation when one module in the system breaks down. In particular, the high productivity of the modular structure will become important in future power electronics systems because the demand for power conversion systems will drastically increase owing to the use of electric energy, e.g., electric vehicles and renewable energy sources. Conventional PEBB modules do not include elements of high-speed controllers, input/output filters, and detection circuits even though these modules consist of main circuits, gate drivers, and passive components [6]. Therefore, user-friendly design and flexibility of systems still have issues because the system controller and the other components, such as the detection unit, have to be developed, as well as the conventional power conversion system without PEBBs.

The USPM concept realizes a power electronics system by stacking power modules according to the rated voltage and current requirements of the modules, similar to the PEBB concept. USPM attempts to improve productivity, expandability, and versatility compared to other modular converter systems. Uniquely, USPM contains all of the power conversion components. Each USPM outputs voltage and current waveforms with low harmonics without the peripheral devices. In particular, the high-speed controller in each USPM has a fast response with a short delay to improve the response performance. Thus, each USPM behaves as a control voltage source or a control current source that outputs arbitrary waveforms from the perspective of the master controller. This controlled power supply operation improves the versatility and usability of the system

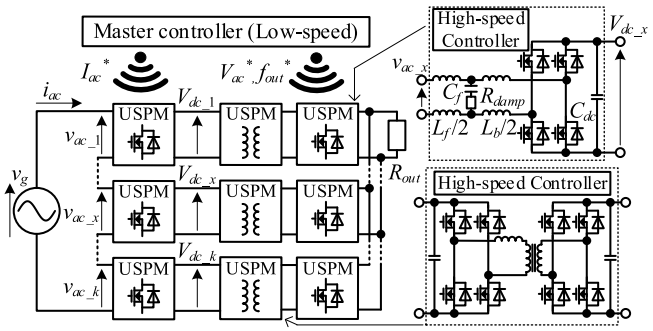

Fig. 2. Configuration of the USPM system. The USPMs in multiple-series and multiple-parallel connections are driven by command values from a low-speed master controller. One candidate for the nonisolated USPM is a full-bridge converter, and one candidate for the isolated USPM is a DAB converter.

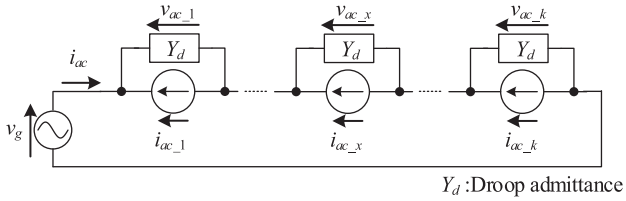

Fig. 3. Equivalent circuit in the current droop control. The interference of each USPM is suppressed by connecting a droop admittance Y_d in parallel to each USPM, which is a current source operation.

to realize various types of power conversion. Voltage-source- and current-source-type USPMs have variations in options, such as rated specifications (e.g., voltage and current), main circuits, and isolation functions, such as analog ICs. Note that circuits with multiple power conversions, such as H-bridge inverters, can easily be changed from the master controller in terms of control method, control target, and power supply type. This variation improves the usability of USPM even further.

USPMs are connected to this configuration in multiple units. This causes system complexity and low reliability because many control signal lines are required. Therefore, this system adopts a wireless system using wireless communication. Wireless communication improves the flexibility of the master controller placement and the reduction of the system volume by simplifying the system, including the control signal lines. However, in the USPM system, high-speed communication does not adopt as a wired system because wireless communication is assumed. Thus, USPM is driven by receiving an effective value command or a frequency command, not an instantaneous value command. The system designer designs each element according to the system specifications when a completely new system is constructed in a conventional modular converter system. However, the design requires trial and error in consideration of noise, heat dissipation, and, e.g., the simulations and the prototype experiments. On the other hand, in the USPM system, the system designer only determines the configuration with USPM and the number of series or parallel connections of USPM. Therefore, the USPM system realizes simplification of the design flow and high productivity, as compared to the conventional PEBB system, because the USPM system is constructed without the need for a dedicated design.

Fig. 2 shows an example of the system configuration in USPM. In this article, a single-phase ac–ac power converter is shown. The primary-side USPM applies the input current control, and the secondary-side USPM applies the output voltage control. These USPMs have the main circuit of the H-bridge, including the *LCL* filter. Furthermore, an isolated USPM is inserted between the primary side and the secondary side to prevent a short circuit. One candidate of the isolated USPMs topology is a dual active bridge (DAB) converter, which is a different circuit configuration of the primary and secondary USPMs. The advantages of a DAB converter are bidirectional power flow and wide zero-voltage switching operation range when the transfer ratio is fixed. As a result, the DAB can achieve very high power density and high efficiency. In other words, the behavior of the isolated USPM is the same as a transformer in the dc line. It is noted that the control response is exactly different between the isolated and nonisolated USPM. Therefore, the droop control in the nonisolated USPM does not affect the parameters of the soft switching operation and high-frequency control in the isolated USPM. Therefore, the USPM system can independently design the input current and output voltage control from the high-frequency component.

The primary-side current control interferes among the series-connected USPMs due to delays and gain errors caused by temperature drift and settling errors of current detection. Thus, the unbalance of the output voltage due to the control interference causes steady-state overmodulation and control failure due to the insufficient dc voltage. In this article, the current droop control is considered in order to solve this problem.

III. Proposed Current Droop Control

A. Theory and Implementation

Fig. 3 shows the equivalent circuit of the current droop control. Note that v_g and i_{ac} are the grid voltage and the grid current, respectively, and subscript x indicates the module number of USPM. The USPM output voltage v_{ac} and USPM output current i_{ac} with subscript x are the values detected by each USPM. The ideal current source in Fig. 3 represents the controlled current source of each USPM that controls the current. Note that the input impedance of USPM and the grid impedance can be neglected because they are very small and do not affect the control performance of the current droop control. The current droop control is in duality with the voltage droop control used in microgrids and other applications. In the current droop control, a virtual droop admittance Y_d is connected in parallel to the current source. Even if i_{ac_x} becomes unbalanced, Kirchhoff's first law can be satisfied because the current i_{ac} minus i_{ac_x} flows into Y_d. In this way, the interference of current sources connected in series is suppressed. The current droop control is obtained by subtracting the droop current from the current command. The droop current is given by

$$i_{ac} = \frac{Y_d v_g}{k} - \frac{1}{k}\sum_{x=1}^{k} i_{ac\_x} \tag{1}$$

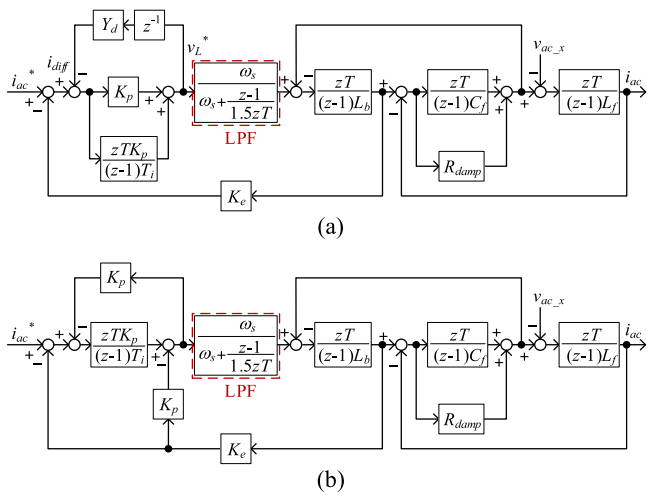

Fig. 4. Control block diagram of the USPM with current control when the current control is configured with the PI and IP controls. The LPF simulates PWM delay and zero-order hold. The PI control has a first-order delay inserted in the current droop control loop to avoid recursive operations, whereas the PI control does not. (a) PI current control. (b) IP current control.

where k is the number of USPMs connected in series. The first term in (1) gives the drooping characteristic to the system current. The voltage v_{ac_x} of each current source under the current droop control is given by the following equation from Fig. 3:

$$v_{ac\_x} = \frac{v_{ac}}{k} + \frac{1}{Y_d}\left(i_{ac} + i_{ac\_x}\right). \tag{2}$$

According to (2), the voltage of each current source is unbalanced when the difference between i_{ac} and i_{ac_x} becomes larger. On the other hand, the overmodulation is prevented by increasing Y_d because the voltage unbalance becomes smaller. Overmodulation is also suppressed by increasing the dc-link voltage because it occurs when the unbalanced voltage is larger than the dc-link voltage.

In the equivalent circuit of Fig. 2, the closed-loop transfer function $i_{ac\_x}(s)/i_{ac}^*(s)$ of the entire system and the ac output voltage characteristic $v_{ac\_x}(s)/i_{ac}^*(s)$ of each module is given by

$$\frac{i_{ac}(s)}{i_{ac}^*(s)} = -\frac{1}{Z_g + \sum_{x=1}^{k}\frac{v_{ac\_x}(s)}{i_{ac\_x}(s)}} \times \left(\sum_{x=1}^{k}\left(\frac{v_{ac\_x}(s)}{i_{ac\_x}(s)}\frac{i_{ac\_x}(s)}{i_{ac}^*(s)}\right) - \frac{v_g(s)}{i_{ac}^*(s)}\right) \tag{3}$$

and

$$\frac{v_{ac\_x}(s)}{i_{ac}^*(s)} = \frac{v_{ac\_x}(s)}{i_{ac\_x}(s)}\left(\frac{i_{ac\_x}(s)}{i_{ac}^*(s)} + \frac{i_{ac}(s)}{i_{ac}^*(s)}\right) \tag{4}$$

where i_{ac_x} and $Y_{d\cdot x}$ corresponds to the closed-loop transfer function $i_{ac\_x}(s)/i_{ac}^*(s)$ and the disturbance rejection characteristics $i_{ac\_x}(s)/v_{ac\_x}(s)$, respectively. The equation for designing the current droop gain is obtained from these characteristics.

The difference between the voltage droop control and the current droop control is the position of its implementation. In voltage droop control, the droop control does not directly affect control performance because the command value of the current control in the latter stage of the voltage control only changes. On the other hand, the inverter voltage feedback by the current droop control is increased or decreased. The current droop control must be designed for Y_d to avoid control failure due to overmodulation because the inverter voltage is limited by the dc-link voltage. In addition, the current droop control has to avoid interference with the voltage control, which is above the current control in the figure when the current droop control is implemented.

Current controls applied to power converters include a proportional (P) control, a PI control, an IP control, a PR control, etc. USPM basically employs controllers that can operate over a wide frequency range from dc to several hundred hertz in terms of general-purpose use. USPMs are widely used for grid-connected inverters, dc–dc converters for batteries, series and parallel active filters, etc. In addition, the USPM can also be used for motor drive applications, i.e., by extending the main circuit. However, the P and PR controls are unsuitable for the current control applied to USPM because they have low robustness in the disturbance characteristics depending on the frequency range. As a result, the PI control and the IP control only are discussed in this article, excluding the P control and the PR control. Note that control methods control can be changed from the master controller depending on the application.

Fig. 4 shows the control block diagram of USPM with the current droop when the current control is configured with proportional-integral (PI) and integral-proportional (IP) control. Note that $i_{\rm diff}$ is the input of the current controller, which is the difference between the current command value and the current detection value, and v_L is the input of the current droop control, which is the inverter voltage command value. According to Fig. 4, a first-order low-pass filter (LPF) is inserted into the output of the current control to emulate the delay caused by pulsewidth modulation (PWM) and detection. Note that K_e is the detection gain error, which is usually 1 p.u., and varies depending on the parameter error of the detection circuit. The current droop control is implemented by the feedback of the current control output, the current droop gain Y_d, and the current command value. In this case, the current droop control by PI controller requires a first-order delay along with Y_d in order to avoid recursive operations.

B. Response Characteristics Analysis

Table I shows the analytical and experimental parameters of the two series-connected control current source modules. In this article, the stability analysis of each controller is considered when the detection error occurs.

Fig. 5 shows the frequency characteristics of the PI controller in the transfer function from the differential current $i_{\rm diff}$ to the estimated voltage of the inductor v_L^* in Fig. 4. According to Fig. 5, the gain characteristics decrease with the increase of Y_d because the low-bandwidth gain by the current droop control is limited. The advantages of responsiveness and disturbance suppression characteristics cease to exist when the gain is reduced to the same as the P control gain. In addition, the gain reduced by

TABLE I
ANALYSIS AND EXPERIMENTAL PARAMETERS

Cell Rated Power (1 p.u.)	P	500 W	Proportional Gain of Current Control	K_p	1.444
Cell Rated AC Voltage (1 p.u.)	V_{ac}	100 V	Integral Time of Current Control	T_i	45.0 μs
Rated AC Current (1 p.u.)	I_{ac}	5 A	Droop Admittance	Y_d	0—0.05 S (0—1.0 p.u.)
Rated admittance (1 p.u.)	Y_n	0.05 S	Voltage Det. Gain	K_e	0.97—1.03
Grid Frequency	f_g	50 Hz	Filter Inductor	L_f	650 μH (%Z:1.02%)
Dc-link Voltage (1 p.u.)	V_{dc}	200 V	Filter Capacitor	C_f	22 μF (%Y:13.8%)
Sampling Frequency (=Switching Frequency)	f_{samp} ($=T^{-1}$)	80 kHz	Boost Inductor	L_b	650 μH (%Z:1.02%)
			Damping Resistor	R_{damp}	2 Ω (%Z:10%)
Dead time	T_d	200 ns	Dc-link Capacitor	C_{dc}	480 μF (H:19.2 ms)

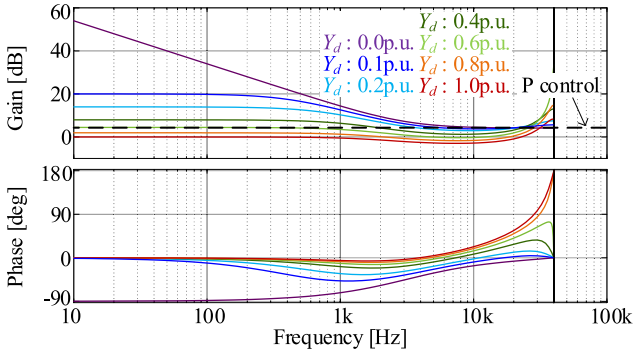

Fig. 5. Bode plots of the transfer function from $i_{\rm diff}$ to v_L^* with PI current control. The gain in the low-frequency range is flat and decreases as Y_d increases due to current droop control.

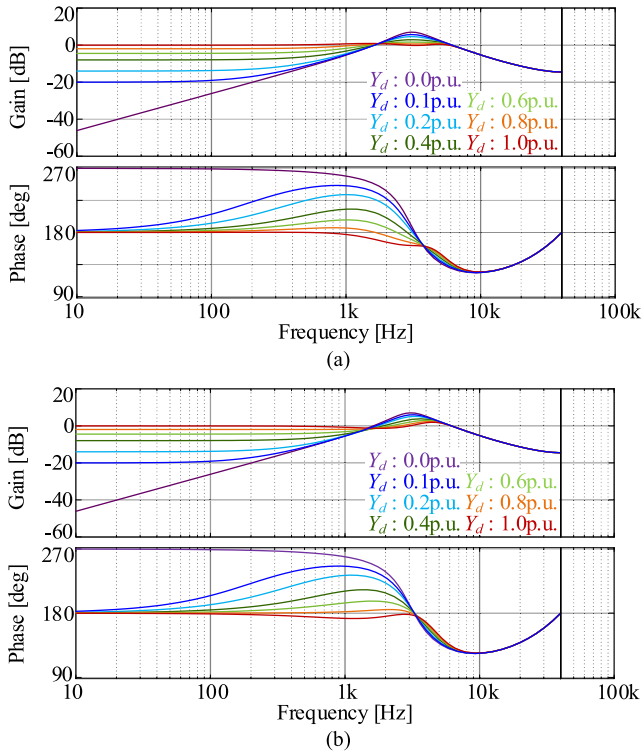

Fig. 6. Bode plots of the transfer function from v_{ac} to i_L. The characteristics in the low-frequency range also becomes worse as Y_d increases for both controllers. In the IP control, the disturbance response in the high-frequency range near the peak is improved by the current droop gain. (a) PI current controller. (b) IP current controller.

the current droop control is already constant approximately at the operating frequency. The value of Y_d is designed by adopting this gain characteristic, which becomes constant. The range of Y_d selections and design methods are described in Section IV. Note that the current control bandwidth must be sufficiently higher than the operating frequency because the ac voltage phase of each USPM shifts due to the gain and phase characteristics not being constant when the current control bandwidth and current droop gain are low.

Fig. 6 shows the closed-loop frequency analysis result between the disturbance of $v_{\rm ac}$ and the actual current of i_L in Fig. 4. According to Fig. 6, the two controllers have little difference because the current droop gain is dominant in the low-frequency range below 1 kHz. Therefore, the disturbance suppression gain is not a factor in controller selection. In addition, the two controllers suppress the disturbance, which is the resonance component, because the gain peak decreases with increasing Y_d.

Fig. 7 shows the closed-loop frequency analysis results between the current command i_{ac}^* and the actual current i_L in Fig. 4. According to Fig. 7, the loop gain of the PI controller improves the overshoot of the transient response by suppressing the resonance when the droop gain is increased. However, the large gain and lag phase near 40 kHz destabilize the system. On the other hand, the droop gain does not affect the closed-loop characteristics and hardly changes the gain characteristics in the case of the PI controller. In addition, the outer voltage control to be implemented in the master controller can be designed without considering the effect of the current droop control because

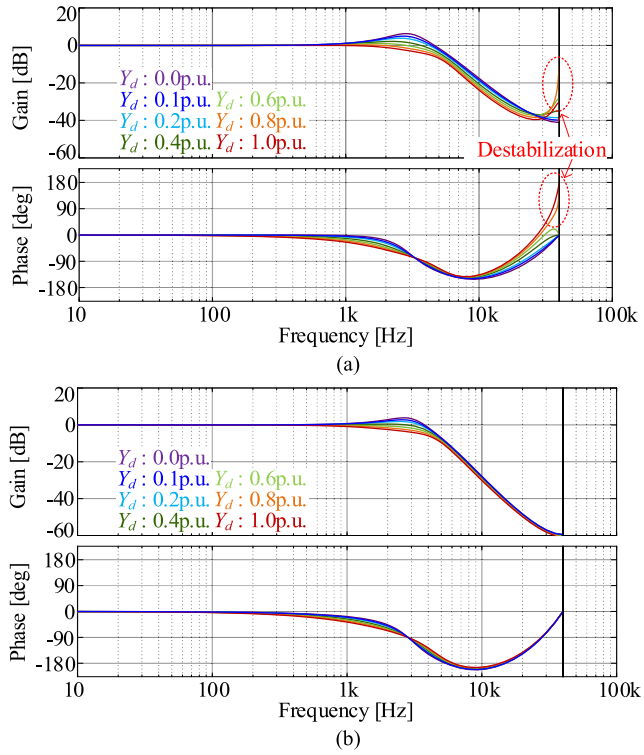

Fig. 7. Bode plots of the transfer function from i_{ac}^* to i_L. The gain characteristics increase around 40 kHz in PI control. IP control has almost no change in the gain and phase characteristics. (a) PI current controller. (b) IP current controller.

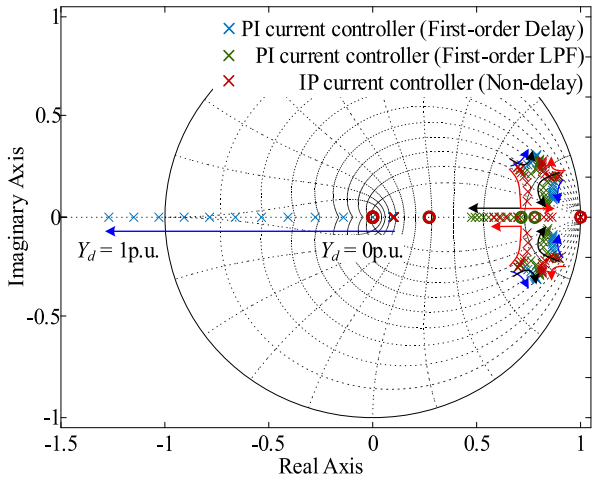

Fig. 8. Root locus of the current control system when the current droop gain is varied. The PI control becomes unstable as the poles move outside the unit circle. IP control is stable because the poles are within the unit circle.

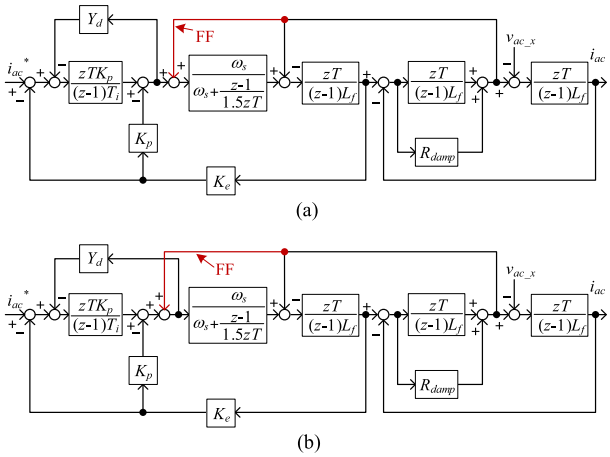

Fig. 9. Block diagram of the current control adopting FF compensation. The current controller has the same disturbance suppression characteristics as the case without the current droop control when FF compensation is performed in Fig. 9(a). The current droop characteristics are the same as those without FF compensation when FF compensation is performed in Fig. 9(b). (a) Outer current droop control loop. (b) Inner current droop control loop.

the wireless communication must have a much lower control bandwidth than the current controller.

Fig. 8 shows the root locus of the current controller adopted with the current droop control in Fig. 4. According to Fig. 8, the pole of the PI controller moves to the outside of the unit circle when the droop gain is increased. The limit of Y_d for stable operation under this condition is 0.78 p.u. The instability caused by droop control is suppressed by reducing L_b. The small L_b is difficult to control due to the impedance between the filter and the output side. Thus, instability is avoided by changing the delay to a first-order LPF in the PI controller. However, the LPF must be designed for each controller because the gain characteristics change around the cutoff frequency. Note that the cutoff frequency of the LPF is set to 5000 Hz in order to avoid a significant reduction in the bandwidth of the current controller. On the other hand, all poles are kept in the unit circle when the IP controller is adopted.

From the results in Figs. 6–8, the USPM system applies an IP controller with the current droop control because IP control is superior to PI control in terms of both responsiveness and stability.

C. Voltage Disturbance Feed-Forward (FF) Compensation

Fig. 9 shows a block diagram of the IP current controller with the voltage disturbance FF compensation. The deterioration of the disturbance suppression characteristics on the low-frequency side is generally compensated by FF compensation of the disturbance voltage to the current control output [16]. However, the FF compensation may affect the current droop control, in which the inverter voltage is the control quantity because the FF compensation is inserted into the inverter voltage. Therefore, the effect of the FF is discussed again. The difference between Fig. 9(a) and (b) is that the FF compensation is placed before or after the inverter voltage command to which the current loop control refers.

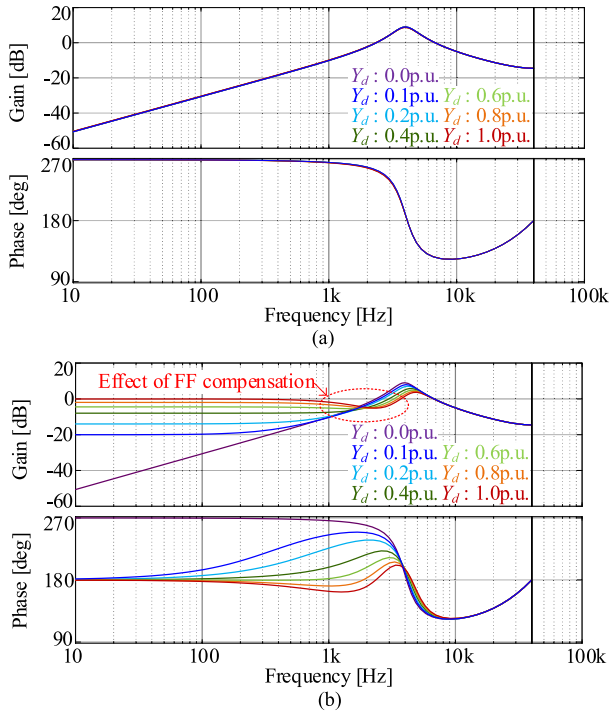

Fig. 10. Bode plots of the transfer function from v_{ac_x} to $i_L$adopting FF compensation. The current controller provides the same disturbance suppression characteristics as that without current droop control when FF compensation is performed in Fig. 10(a). The disturbance suppression characteristics at 1–4 kHz are only slightly improved by the effect of FF compensation when FF compensation is performed in Fig. 10(b). (a) Outside current droop control loop. (b) Inside current droop control loop.

Fig. 10 shows a bode plot of the transfer function from v_{ac} to i_L when FF compensation is adopted. According to Fig. 10(a), the current controller provides the same disturbance suppression characteristics as that without current droop control when FF compensation is performed in Fig. 9(a). However, the effect of the current droop control is not achieved because the feedback

voltage in Fig. 9(a) is the estimated voltage of the inductor. On the other hand, according to Fig. 10(b), the effect of the current droop control is achieved because the feedback voltage in Fig. 9(b) is the inverter voltage. The effect of the FF compensation with increasing disturbance gain appears slightly near the resonance peak around 1–4 kHz, where the characteristics of the current droop control are not dominant, in the disturbance suppression performance. Unfortunately, the disturbance suppression gain in the low-frequency range, such as the grid frequency controlled by USPM, is equivalent to that without FF compensation.

Here, Y_d should be less than 0.1 p.u. because the actual detection gain error is approximately $\pm 3\%$ at most. According to Fig. 10(b), the disturbance voltage is suppressed sufficiently under the condition of $Y_d = 0.1$ p.u. or less because the disturbance suppression gain in the low-frequency range is more than -20 dB. Therefore, the current droop control suppresses the effect of the disturbance by setting the droop gain appropriately without FF compensation.

The analysis in Fig. 10 shows that the USPM cannot get good performance in terms of both disturbance suppression performance and decoupling by current droop control. Therefore, the USPM that applies current droop control does not employ voltage disturbance FF compensation.

IV. Design and Simulation

A. Design of Current Droop Control Gain

In current droop control, the current deviation δI must be as small as possible within the specification from the viewpoint of power converter protection and highly responsive control because the ac current changes due to droop characteristics. The unbalance of the ac and dc voltages due to the interference of each current source module causes intermittent overmodulation and control failure. This condition is unique to the current droop control, where the output of the current control is the voltage command of the inverter. Y_d must be designed to satisfy both conditions.

The proposed design method is obtained by solving the transfer function at 0 Hz because the gain characteristics become flat in the low-frequency range around the operating frequency shown in Fig. 5. Thus, the design method assumes that the controller has a current control bandwidth that is sufficiently higher than the operating frequency, as in USPM. The current source and parallel resistance on the equivalent circuit are given by

$$\frac{i_{ac\_x}(s=0)}{i^*_{ac}(s=0)} = \frac{1}{K_{e\_x}} \tag{5}$$

and

$$\frac{i_{ac\_x}(s=0)}{v_{ac}(s=0)} = -\frac{Y_d}{K_{e\_x}}. \tag{6}$$

Equations (5) and (6) are easily obtained using the detection gain and current droop gain. The lower and upper limits of the current droop gain are obtained by adopting (3) and (4) to (5) and (6), as follows:

$$Y_d[p.u.] \le \left((1+\delta I)\frac{\sum_{y=1}^{k} K_{e\_y}}{k} - 1 \right) \frac{R_n}{R_{out}} \tag{7}$$

and

$$Y_d[p.u.] \ge \frac{\left(K_{e\_x} - \frac{\sum_{y=1}^{k} K_{e\_y}}{k} \right)}{\frac{V_{dc\_\min}}{V_{ac\_\max}} \frac{\sum_{y=1}^{k} K_{e\_y}}{k} - K_{e\_x}} \frac{R_n}{R_{out}} \tag{8}$$

where R_n is the rated impedance of the module and $R_{\rm out}$ is the output impedance of the module. The current droop control achieves high responsiveness without overmodulation by ensuring that all control current source modules satisfy (7) and (8). There are two main design guidelines for Y_d: a design that makes the current response characteristic highly responsive (Case 1) and a design that makes the detection error range wide (Case 2). In Case 1, Y_d is set as follows to achieve the critical condition in (7):

$$Y_d[p.u.] = \frac{\left(K_{e\_x} - \frac{\sum_{y=1}^{k} K_{e\_y}}{k} \right)}{\frac{V_{dc\_\min}}{V_{ac\_\max}} \frac{\sum_{y=1}^{k} K_{e\_y}}{k} - K_{e\_x}} \frac{R_n}{R_{out}}. \tag{9}$$

In Case 2, Y_d is set as follows so that (7) is equal to (8):

$$Y_d[p.u.] = \left(\frac{\frac{V_{dc\_\min}}{V_{ac\_\max}} - 1 + (1-E_{rr})(1+\delta I)}{\frac{V_{dc\_\min}}{V_{ac\_\max}}} - 1 \right) \frac{R_n}{R_{out}}. \tag{10}$$

In this design method, the upper limit of the number of modules exists, although it is not strictly determined. The module number is limited for two reasons as follows.

1) The voltage isolation of the USPM hardware design will be designed toward a low voltage (200–400Vac) application to maintain general-purpose use. The maximum voltage of the power conversion system with the USPM will be up to 2 kV because this kind of application has a large volume. Then, the module number will be five.
2) The overmodulation is caused by the current droop gain, which is determined from the deviation of the detection error and the margin of the modulation index. Therefore, the overmodulation will occur when the system has large detection errors or no margin of the modulation index due to low dc voltage compared with the ac-side voltage. That is, the module number will be increased when the USPM uses the low detection error current sensors ($< \pm 3\%$) and a large margin of modulation index. It is noted that the module number limitation depends on the design of the USPM. Therefore, if the specific USPM is designed for modular multilevel cascade converter in medium-voltage applications, then the module number will increase.

Following the aforementioned design guidelines, Y_d was set to 0.078 p.u. in Case 1 with a detection error of $\pm 3\%$ in order to achieve high responsiveness.

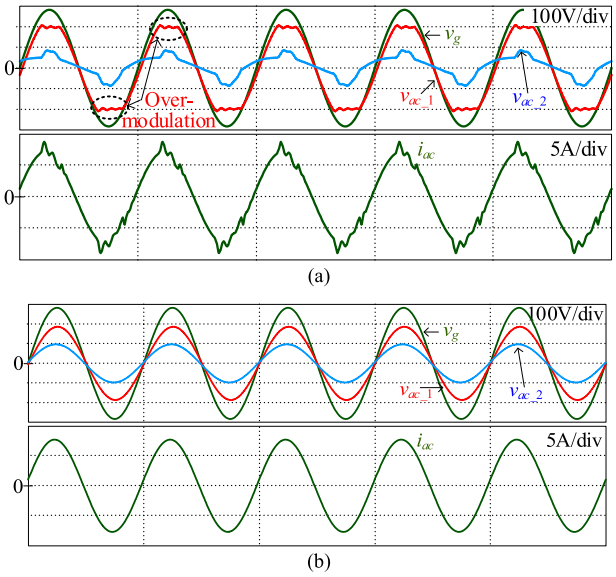

Fig. 11. Simulation results when current droop control is adopted. Current waveforms are distorted by overmodulation when the current droop gain is small. The system is operating without overmodulation due to appropriate gain design. (a) $Y_d = 0.005$ p.u. (b) $Y_d = 0.078$ p.u.

B. Simulation of Proposed Design Method

This section verifies the validity of the theoretical equations and the behavior when decoupling by current droop control is not possible. Note that USPM applies the IP control in Fig. 4(b). The instantaneous current command i^*_{ac} is the sum of the rms current command value from the master controller and the sine wave using the phase information applied to the ac-side voltage of each USPM by the PLL.

Fig. 11 shows the simulation results for the conditions of $Y_d =$ 0.005 p.u. (small current droop gain) and $Y_d = 0.078$ p.u. Under the condition of $Y_d = 0.005$ p.u., one of the current controllers is overmodulated because the amplitude of the ac voltage is larger than the dc-link voltage. This overmodulation is caused by the unbalance of the output of each USPM due to the detection gain error. Therefore, the overmodulation should be avoided by adopting robust PLL and the current droop control in order to lose the phase-locked loop (PLL) operation in each USPM. This overmodulation is avoided by adopting robust PLL and current droop control. Here, the current total harmonic distortion (THD) is 9.1%. Under the condition of $Y_d = 0.078$ p.u., the ac current THD is 0.30% because the ac voltage barely avoids overmodulation near the dc-link voltage. The current deviation under this condition is 8.8%, which corresponds to a current error of 0.93% from the calculated equation.

These results demonstrate that current droop control suppresses interference among series-connected USPMs and the theoretical equation is valid.

V. Experimental Results

The actual equipment verification in this section demonstrates the characteristics of current droop control revealed in Sections III and IV.

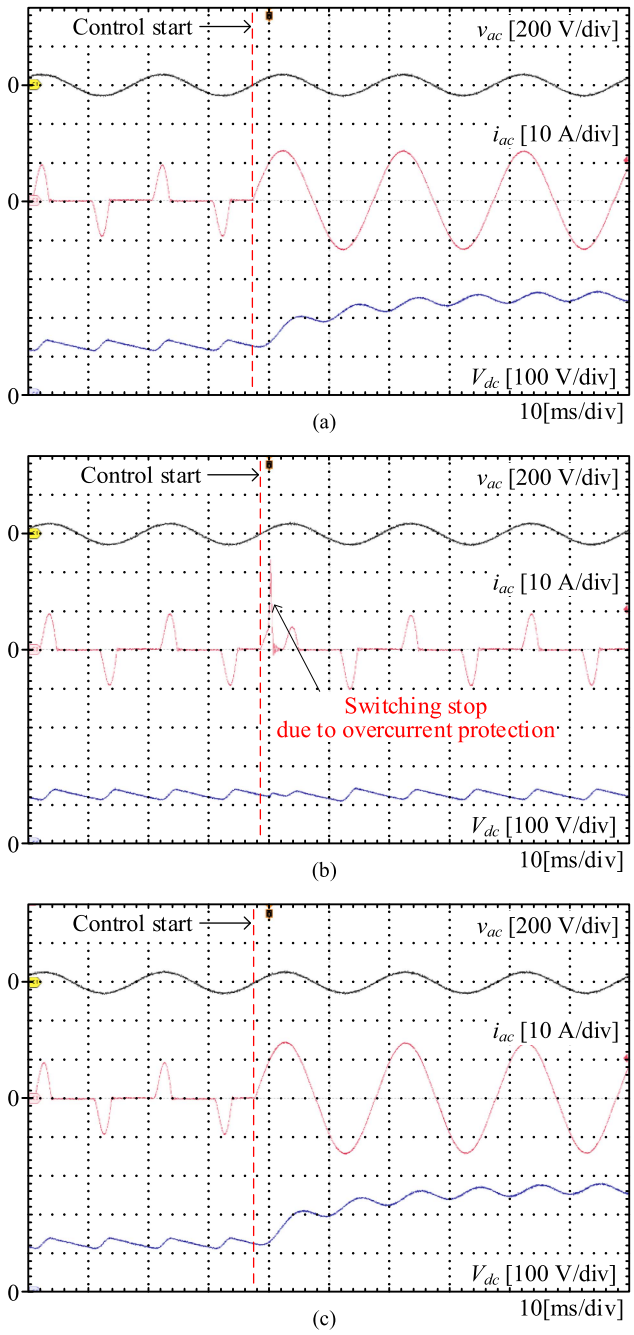

Fig. 12. Startup operation waveforms under each control condition. The PI control stops working when Y_d increases due to overcurrent. IP control works stably even when Y_d is 1 p.u. (a) PI current controller ($Y_d = 0.76$ p.u.). (b) PI current controller ($Y_d = 0.77$ p.u.). (c) IP current controller ($Y_d = 1.00$ p.u.).

Fig. 12 shows the experimental results when the converter is started at each controller and Y_d. Note that USPM applies the PI or IP control shown in Fig. 4 to verify the stability range of each control. According to Fig. 12, the converter with the PI controller works stably when Y_d is 0.76 p.u. However, the operation is not kept due to overcurrent protection when Y_d changes to 0.77 p.u. The stable analysis results in Fig. 8 are matched with the experimental results with an error of 1.3%. The cause of the error in the unstable Y_d is the error in the detection

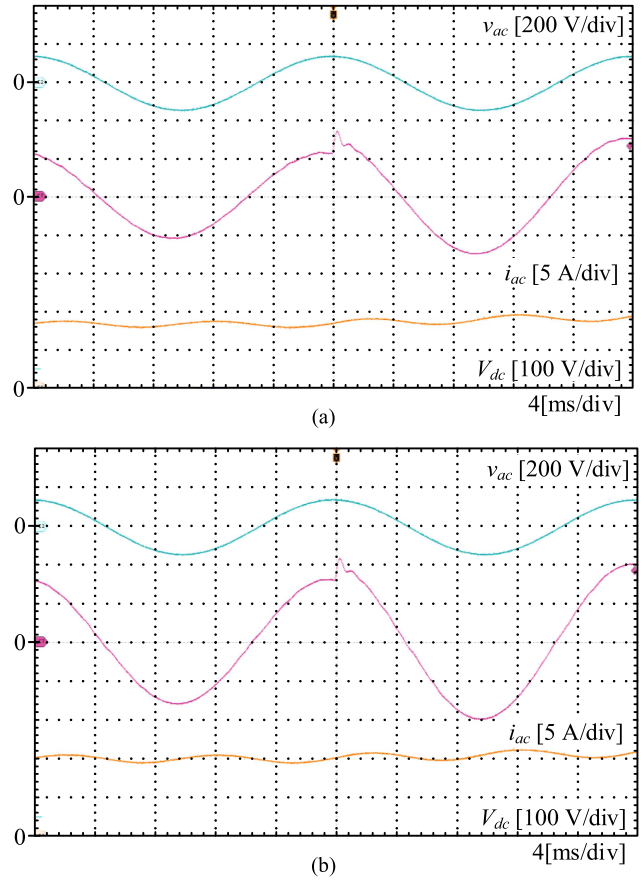

Fig. 13. Experimental waveform when the command value is varied. The transient response is almost unchanged, although the rms current value changes with the increase of Y_d. (a) $Y_d = 0.10$ p.u. (b) $Y_d = 0.50$ p.u.

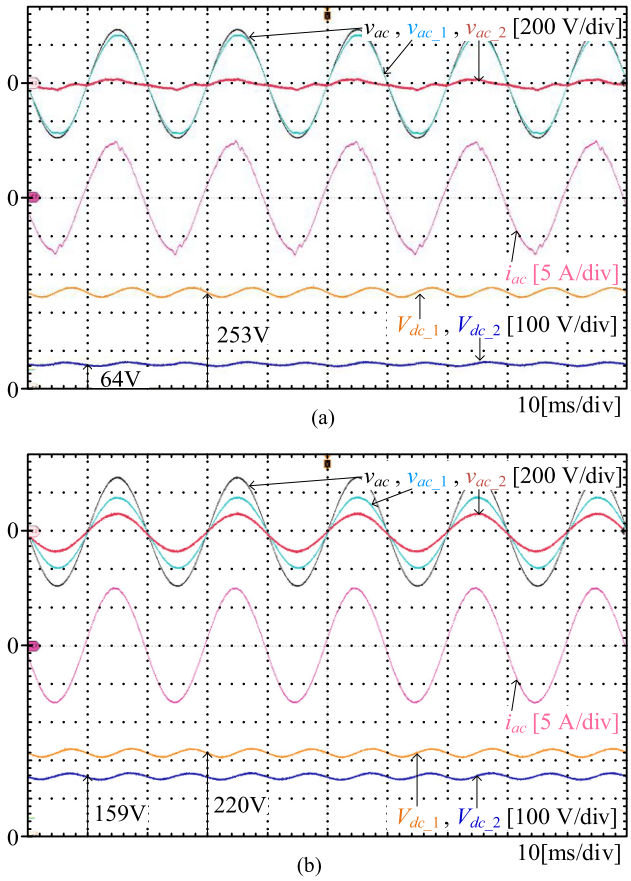

Fig. 14. Effect of FF compensation outside the current droop control loop. The voltage is unbalanced due to the interference of the current controller, although the current value follows the command value by FF compensation. (a) With FF compensation. (b) Without FF compensation.

delay and inductance. On the other hand, the converter using the IP controller is stable even when Y_d is 1 p.u. This experiment demonstrates that IP control is more suitable for the current droop control than PI control.

Fig. 13 shows the ac current waveform when the command value is changed in steps from 0.7 to 1 p.u. at $Y_d = 0.1$ and 0.5 p.u. Note that the target response of USPM applying IP control with droop control in Fig. 4(b) has been verified. According to Fig. 13, the current rms values are different due to the droop characteristics shown in (1). In the experiment with $Y_d = 0.1$ p.u., the current rms value is 3.96 A at 0.7 p.u. and 5.30 A at 1 p.u., which agrees with the theoretical equation with an error of 4.0% or less. On the other hand, the transient response is consistent regardless of Y_d. Therefore, the current droop control is not the cause of limiting the bandwidth of the upper control system.

Fig. 14 shows the operating waveforms at rated operation when the FF compensation in Fig. 9(a) is adopted. Here, Y_d is set to 0.078 p.u. based on the design equation of (9). In this experiment, the effect of the FF compensation in Fig. 9(a) on the noninterference property of the current droop control is verified. The unbalance is intentionally generated by increasing the current detection gain of the USPM by +3% and -3% in order to check the effect of the current droop control. According to Fig. 14(a), the voltage unbalance is improved without FF compensation in Fig. 9(b) at the expense of the increase in ac current. The current THD is reduced to 0.9% by balancing the ac and dc voltages. Here, the current deviation is 5.46%, which agrees with the analyzed value with an error of 2.17%. The main reason for the error is that there was originally a detection gain error in the detection circuit. Moreover, the ac voltage unbalance ratio is 30.7%. Therefore, control to match the power to the outer loop is required because the voltage amplitude is impossible to perfectly balance with the current droop control alone. On the other hand, the ac and dc voltages are unbalanced due to insufficient current droop control. Here, the dc voltage unbalance ratio is 83.9%. The current THD is 3.1% because the dc-link voltage cannot be maintained on one side due to this unbalance. In addition, another factor in determining that the system is not sufficiently decoupled is that there is no positive current deviation with rms current value of 0.98 p.u. Therefore, the FF compensation in Fig. 9(a) is not suitable for the current control applying the current droop control.

Fig. 15 shows the operating waveforms during the system voltage drop and recovery when the FF compensation in Fig. 9(b) is adopted. Note that the system voltage drops from 2 to 1 p.u. at the maximum positive voltage. Moreover, Y_d is set to 0.078 p.u. as in Fig. 14. This experiment demonstrates the effect

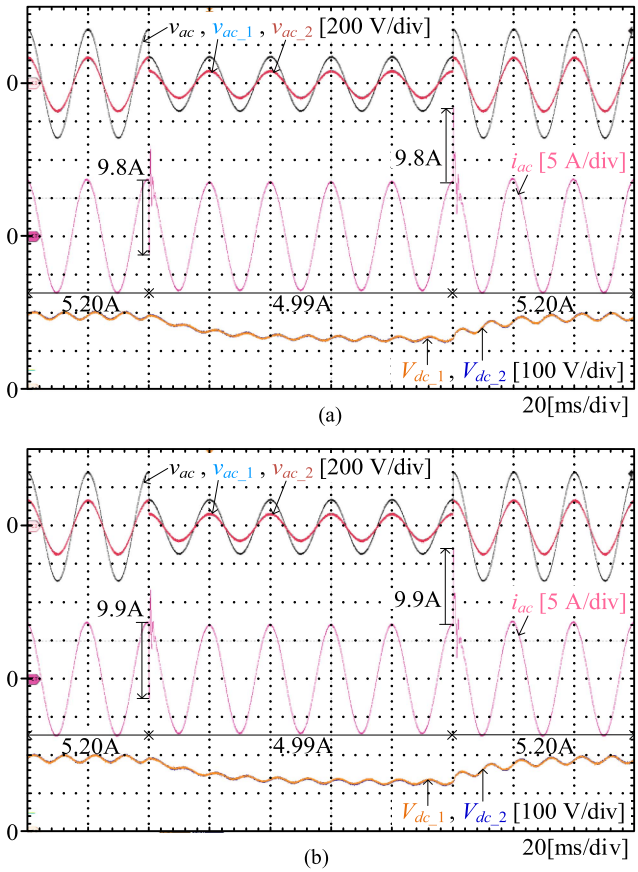

Fig. 15. Effect of FF compensation in the current droop control loop. The rms current value with FF does not change compared to that without FF compensation. The current deviation of 5% at the rated voltage indicates that the disturbance is sufficiently suppressed. (a) With FF compensation. (b) Without FF compensation.

of the FF compensation in Fig. 9(b) for current droop control on noninterference. According to Fig. 15, the disturbance of the system frequency component is not completely removed by FF compensation in Fig. 9(b) because the current amplitude is reduced from 1.04 to 1.00 p.u. when the system voltage drops with or without FF compensation. However, the current controller is able to suppress the disturbance sufficiently because its current deviation is 4.0%. Moreover, the large current change occurring at the moment of voltage fluctuation is independent of the droop control because the current change is a high-frequency component. This large current change is reduced by the appropriate design of the current controller because the small filter inductor causes this change. Consequently, the FF compensation in Fig. 9(b) is unsuitable because it does not provide sufficient disturbance suppression performance even if the current control employs the current droop control.

VI. Conclusion

This article proposed a current droop control method to be adopted to each series-connected current source module of a new autonomous distributed power conversion system. This system was developed to shorten the development time by simplifying the design in power conversion systems. The gain of the current droop control was designed to be stable and highly responsive in order to achieve multiple series of current source modules. In addition, the IP controller was found to be suitable for the current controller adopting the current droop control. The power conversion system is able to increase the voltage capacity easily by implementing the proposed control. Investigations using wireless communication and voltage control by the master controller are planned to be considered for high-accuracy power sharing.

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