Achievement of 6.78-MHz and 3-kW Single Inverter in Continuous Operation

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***Abstract*-- This paper proposes a design flow and implementation method of a high-frequency and high-power inverter for wireless power transfer(WPT) systems. This design flow is revealed to achieve zero-voltage-switching (ZVS) operation and lower the thermal resistance for 3-kW continuous operation in 6.78 MHz. The printed circuit board(PCB) and a dead time design are theoretically described to achieve ZVS operation. In addition, the performance of a heat dissipation structure for a surface-mounted device(SMD) is evaluated by comparison of three types of heat dissipation structures to reduce the thermal resistance effectively. As a result, the continuous operation of the inverter is demonstrated with a 3.3 kW prototype at 6.78-MHz in experimental.**

***Index Terms*—high-frequency inverter, wireless power transfer, zero voltage switching, thermal design**

I. Introduction

Recently, battery chargers have been installed widely for Electric Vehicles (EVs). Notably, WPT systems for battery chargers have been actively studied for safety and convenience [1–2]. So far, the WPT system for the EV charger is normalized to 85 kHz. Although, the weight of the transfer coil becomes heavy at 85 kHz. Thus, the WPT system with megahertz, which is 6.78-13.56 MHz as an industrial scientific and medical(ISM) band, has been actively studied [3–6] to reduce the weight and volume of the system. In order to achieve the megahertz switching, a GaN device is usually employed in the circuit for the WPT system [7–8].

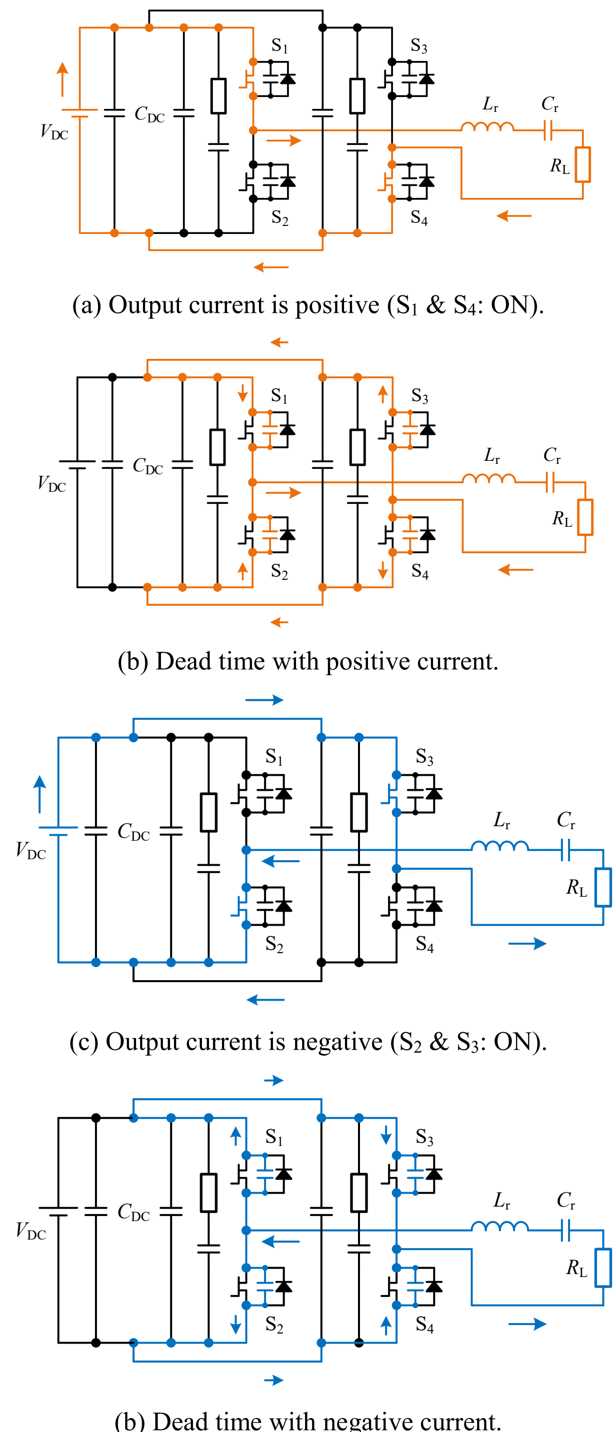
However, the design and implementation of the circuit, which employs a GaN device with megahertz operation, require much knowledge and know-how about the design of high-frequency circuits. Thus, the design and implementation are complex and unclear to achieve the kilo-watts output with megahertz operation.

This paper proposes the design flow and implementation method of the inverter circuit, which has a kilo-watt output in the megahertz range. This design flow conducts the optimization drive condition of the GaN device with the zero-voltage switching (ZVS) and the safety junction temperature in the megahertz operation. Finally, the validity of design flow and circuit implementation is demonstrated by experiment using a 3.3-kW prototype.

II. Current Path and Width Design

A. Current path on PCB

Figure 1 shows the current path of the full bridge



(a) Output current is positive (S_1 & S_4: ON).

(b) Dead time with positive current.

(c) Output current is negative (S_2 & S_3: ON).

(b) Dead time with negative current.

Fig. 1. Current flow of full-bridge inverter.

inverter for a WPT system. The output side of the inverter is connected to the RLC resonant circuit as the WPT system. Figure 2 shows the ideal switching pattern of devices, drain-source voltage, and output current. The phase delay of the output current is required to achieve the ZVS operation of each device.

The charging and discharging current of the output capacitance of devices flows between both legs during the dead time. Thus, the DC-link should be implemented to decrease the loop area, which consists of both legs and the DC-link wiring on the PCB, because the loop inductance affects output voltage and current.

B. Pattern width of Current path

A skin-effect should be considered when designing the pattern width on PCB because the parasitic resistance of wiring increases, especially in the megahertz band. The skin depth δ is expressed as

$$\delta = \sqrt{\frac{\rho}{\mu \pi f}} \quad (1),$$

where ρ is the electric resistivity, μ is the magnetic permeability, and f is the frequency. Then, the skin depth δ is approximately 24 μm under the following conditions: the frequency f is 6.78 MHz, the electric resistivity of the copper ρ is 16-nΩ·m, the magnetic permeability of the copper is $4\pi\times10^{-7}$ H/m, which is the same as the magnetic permeability in a vacuum.

The minimum wiring width considered the skin depth is determined as

$$w = \frac{1}{2\delta}\left(S_{\text{pattern}} + 4\delta^2\right) - d_{\text{pattern}} \quad (2),$$

where w is the minimum wiring width on the current path, S_{pattern} is the minimum cross-sectional area required to flow the maximum current of the wiring on the PCB, and d_{pattern} is the thickness of the PCB pattern. Then, the minimum wiring width w is 11.2 mm under the following conditions: the minimum cross-sectional area S_{pattern} is 0.53-mm^2, and the thickness d_{pattern} is 70 μm.

III. ZVS Operation of Devices

The importance of ZVS operation is very high in achieving a continuous operation with over a few kilowatts output in the megahertz band. Then, the output current of the inverter is expressed as

$$i(t) = I_{\text{peak}} \sin(\omega t + \phi) \quad (3),$$

where I_{peak} is the amplitude of the output current and ϕ is the phase of the output current. Then, the charge amount at the output capacitance of each device during the dead time is expressed as

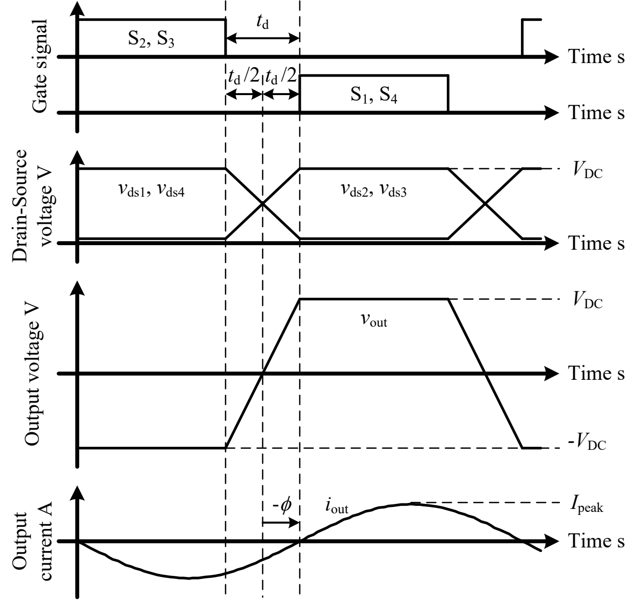


Fig. 2. Current flow and ZVS operation.

Table 1. Simulation parameters.

Main circuit		
DC link voltage	V_{DC}	300 V
Switching frequency	f_s	6.78 MHz
Parasitic capasitance at drain-source of GaN-FET	C_{ds}	130 pF
Load		
Resonant inductance	L_r	6.0 μH
Resonant capacitance	C_r	100 pF

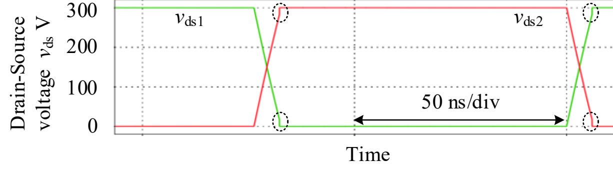
$$Q = \frac{1}{2}\int_{-t_d/2}^{t_d/2} i(t)\,dt = \frac{V_{\text{DC}}}{\pi^2 f Z_L}\sin(\phi)\sin(\omega t_d) \quad (4),$$

where V_{DC} is the DC-link voltage, Z_{L} is the impedance of the RLC resonant load, and t_{d} is the dead time. Then, the minimum value of dead time to achieve ZVS operation is expressed as

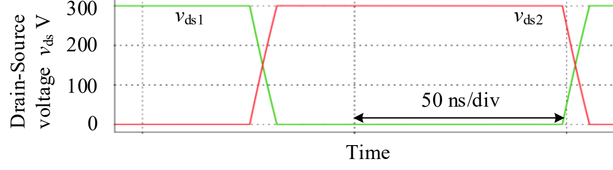
$$t_d = \frac{1}{\omega}\sin^{-1}\left(\frac{\pi^2 f Z_{\text{L}} Q_{\text{oss}}}{V_{\text{DC}}\sin(\phi)}\right) \quad (5).$$

The validity of (5) is checked by simulation. Table 1 shows the simulation parameters. An additional capacitor C_{ds} is connected in parallel to the ideal switch as the parasitic capacitance.

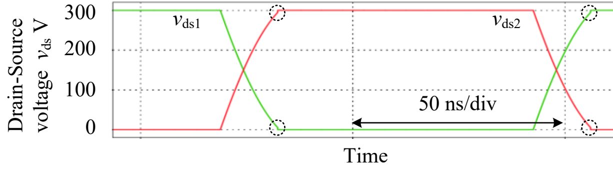
Figure 3 shows the simulation result of the ZVS operation based on the (5). The ZVS operation is achieved when the dead time value satisfies the minimum value calculated by (5). Thus, the equation of minimum dead time value (5) is valid for achieving the ZVS operation.



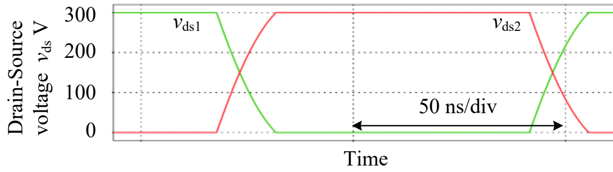
(a) R_L: 15 Ω, dead time: 6.0 ns (Designed: 6.5 ns).



(b) R_L: 15 Ω, dead time: 7.0 ns (Designed: 6.5 ns).



(c) R_L: 30 Ω, dead-time: 13.5 ns (Designed: 14.0 ns).



(d) R_L: 30 Ω, dead-time: 14.5 ns (Designed: 14.0 ns).

Fig. 3. Simulation result of ZVS operation.

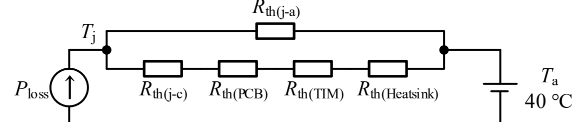
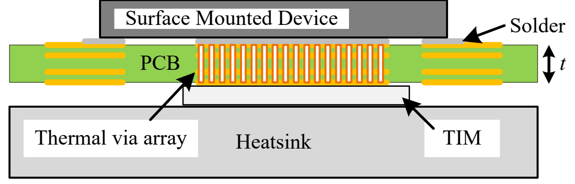
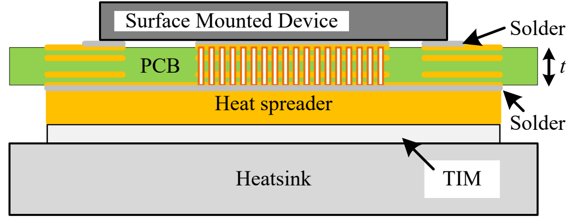


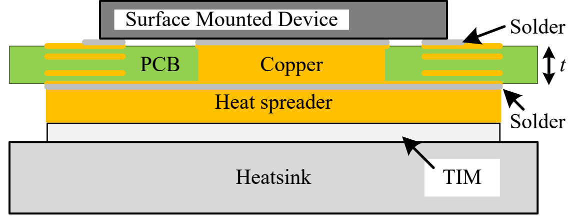
Fig. 4. Equivalent thermal resistance.



(a) Thermal via only.



(b) Thermal via with heat spreader.



(c) Copper block with heat spreader.

Fig 5. Thermal structure on PCB.

IV. Thermal Design of Devices

An optimum thermal design of devices is also essential to continuously achieve a high-frequency and kilo-watt operation because the thermal pad of the GaN device is tiny. Figure 4 shows the thermal resistance circuit of devices. Then, the $R_{th(PCB)}$ is the thermal resistance at the PCB, and the $R_{th(TIM)}$ is the thermal resistance of the thermal interface material. Then, the total thermal resistance is expressed as

$$\left(R_{th(PCB)} + R_{th(TIM)} + R_{th(Heatsink)}\right) = \frac{k_t T_{jmax} - T_a}{P_{Loss}} - R_{th(j\text{-}c)} \qquad (6),$$

where T_a is the ambient temperature, T_{jmax} is the absolute maximum value of the junction temperature, k_t is the temperature margin coefficient, and P_{Loss} is the loss value of each device.

The effective implementation of the thermal resistance is investigated by comparing three cases of the thermal configuration. Figure 5 shows the side view of each thermal configuration. Then, the thermal resistance of PCB and TIM are expressed as

$$R_{th_a,b(PCB\&TIM)} = \Phi_{via} + \frac{d_{TIM(a)}}{k_{TIM}\left(w_{TIM(a)} \times l_{TIM(a)}\right)}$$

Table 2. Parameters of thermal components.

Thermal conductivity of copper	k_{Cu}	393 W/(m·K)
Thermal conductivity of solder	k_{Solder}	57.3 W/(m·K)
Thermal conductivity of air	k_{Air}	0.026 W/(m·K)
Diameter of thermal via	ϕ	0.3 mm
Thickness of the via	d_{PTH}	15 μm
Thickness of the PCB	d	1.6 mm
Number of via	N_{via}	45
Thickness of cupper block	d_{Cu}	1.5 mm
Width of cupper block	w_{Cu}	3.0 mm
Length of cupper block	l_{Cu}	10 mm
Thermal conductivity of TIM	k_{TIM}	3.5 W/(m·K)
Thickness of TIM (a)	$d_{TIM(a)}$	0.7 mm
Thickness of TIM (b & c)	$d_{TIM(b,c)}$	0.6 mm
Width of TIM (a)	$w_{TIM(a)}$	5.0 mm
Width of TIM (b & c)	$w_{TIM(b,c)}$	25 mm
Length of TIM (a)	$l_{TIM(a)}$	10 mm
Length of TIM (b & c)	$l_{TIM(b,c)}$	25 mm
Thickness of heat-spreader	$d_{spreader}$	2.0 mm
Width of heat-spreader	$w_{spreader}$	25 mm
Length of heat-spreader	$l_{spreader}$	25 mm

$$R_{\text{th_c(PCB\&TIM)}} = \frac{d_{\text{Cu}}}{k_{\text{Cu}}\left(w_{\text{Cu}} \times l_{\text{Cu}}\right)} + \frac{d_{\text{spreader}}}{k_{\text{Cu}}\left(w_{\text{spreader}} \times l_{\text{spreader}}\right)} + \frac{d_{\text{TIM(b,c)}}}{k_{\text{TIM}}\left(w_{\text{TIM(b,c)}} \times l_{\text{TIM(b,c)}}\right)}$$

where d is the thickness, w is the width, l is the length, k is the thermal conductivity of each material, and Φ_{via} is the thermal resistance of the thermal via. Table 2 shows each parameter of thermal components. The thermal resistance Φ_{via} is calculated by [9].

Figure 6 (a) shows the PCB board, which is used in thermal measurement, and (b) shows the measurement configuration of the thermal resistance. The PCB board has a footprint of a GaN-device PGA26E07BA(600V, 26A, 150℃: Panasonic) and each thermal structure. A heater is applied on the top side of the PCB to get a thermal flow. Then, the thermal resistance is calculated by the thermal flow and the temperature difference.

Figure 7 shows the design and measurement value of the thermal resistance. Then, the filled material in the thermal via directly affects thermal resistance. In the case of the thermal via filled-in solder, the thermal resistance differs by about 24% compared to the case of the air.
In the thermal design, case (c) achieves a 95% decrease in thermal resistance compared to case (a). In the measurement, case (c) also achieves a 92% decrease in thermal resistance.

V. Experimental Verification

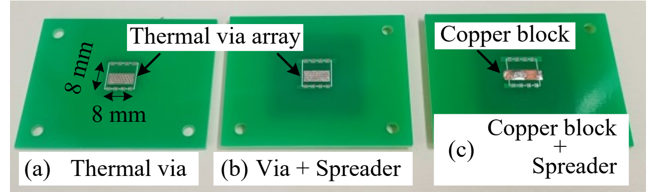
Figure 8 shows the prototype circuit for 6.78 MHz operation. The design of the current path and the thermal implementation are applied to the prototype inverter. The PGA26E07BA is employed as the GaN device.

Table 3 shows the experimental condition. The DC-link voltage in the experiment is 350 V. Then, the output charge of the GaN FET Q_{oss} is 42 nC from the datasheet. The minimum deadtime t_{d} based on the (5) is 6.6 ns.

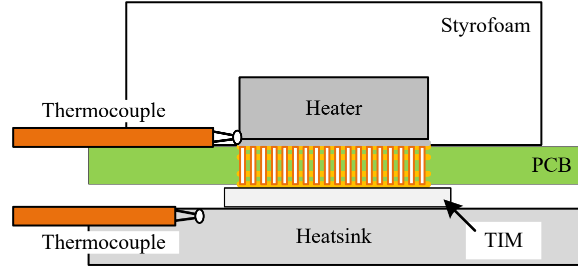
Thermal condition is the same as the thermal measurement. The copper block and the heat spreader are used in each device as the thermal structure Fig.5 (c). The force air cooling is applied to the heatsink.

Figure 9 shows the experimental waveform of the prototype circuit. The input power of the DC-side is 3.4-kW, and the calculated output power based on the measurement waveform is 3.3 kW. Thus, the circuit efficiency achieves 96%.

The ZVS is achieved of devices. However, the minimum dead time value to achieve the ZVS operation is larger than the calculation about three times in the experiment. One of the main causes is the parasitic capacitor between each device and the heat spreader. The required current to achieve ZVS operation increases when the parasitic capacitor becomes large because a part of the load current charges and discharges to the parasitic



(a) Measurement board.



(b) Measurement structure.

Fig. 6. Thermal resistance measurement.

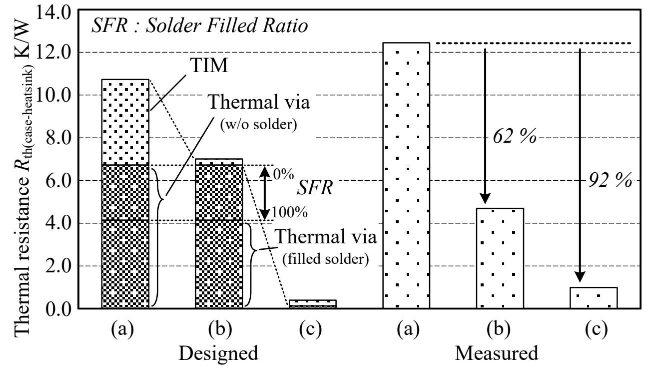


Fig. 7. Measurement result of thermal resistance.

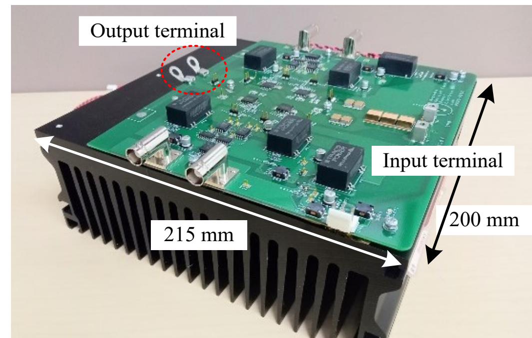


Fig. 8. Prototype circuit operated in 6.78 MHz.

Table 3. Experimental condition.

Main circuit		
DC link voltage	V_{DC}	325 V
Switching frequency	f_{s}	6.78 MHz
Output charge of GaN-FET	Q_{oss}	42 nC
Load		
Resonant inductance	L_{r}	5.8 µH
Resonant capacitance	C_{r}	100 pF
Load resistance	R_{L}	16.7 Ω

capacitor.

Figure 10 shows the temperature on the package of the GaN device for one hour with continuous operation at 6.78 MHz. The package temperature saturates approximately 87℃. The temperature result indicates that the continuous operation of the prototype is stable and safe at 6.78 MHz without a water cooling system.

VI. Conclusion

This paper mentioned a design flow and implementation to achieve a continuous operation with a 3-kW class output in a 6.78 MHz band for a WPT system.

The current path and the skin effect should be considered in PCB design to reduce the influence of the parasitic components and the conduction loss. The skin depth determines the minimum width of the current path. The skin depth is approximately 24 µm in the case of the 6.78 MHz. Then, the minimum width was 11.2 mm for this consideration.

Moreover, the dead time design of the devices is necessary to achieve the ZVS operation. The minimum dead time to achieve the ZVS is derived from the device's output charges and load condition. The validity of the dead time equation was checked by the simulation. The required dead time is 6.6 ns in the experimental condition.

Furthermore, an optimization of the thermal design for the PCB is also needed to reduce the thermal resistance because the thermal pad on the GaN device is very tiny. The thermal resistance of the TIM decreased with a heat-spreader. The thermal resistance of the PCB decreased by a copper block instead of the thermal via array. The heat-spreader and copper block decreased the thermal resistance between the device package and the heatsink by over 90%.

Finally, the prototype circuit based on the design flow and implementation achieved 3.3 kW continuous operation at 6.78 MHz without water cooling.

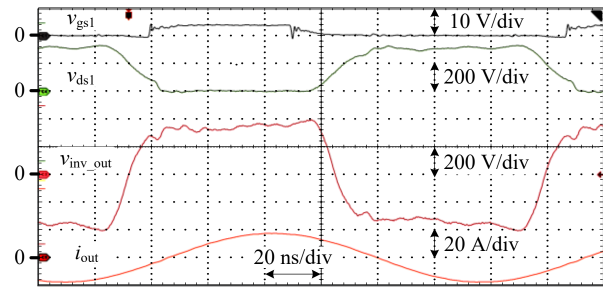


Fig 9. Experimental waveform.

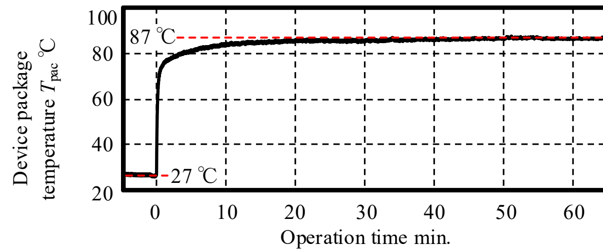


Fig. 10. Temperature of device package.

References

[1] J. Li and D. Costinett, "Comprehensive Design for 6.78 MHz Wireless Power Transfer Systems", 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 906-913.

[2] N. K. Trung, T. Ogata, S. Tanaka, and K. Akatsu, "Attenuate Influence of Parasitic Elements in 13.56-MHz Inverter for Wireless Power Transfer Systems," in IEEE Transactions on Power Electronics, vol. 33, no. 4, pp. 3218-3231, April 2018.

[3] S. Suzuki, T. Shimizu, "A Study on Efficiency Improvement of High-frequency Current Output Inverter Based on Immittance Conversion Element," IEEJ Journal of Industry Applications, 2015, vol 4, no.3, pp. 220-226.

[4] M. Fu, Z. Tang, and C. Ma, "Analysis and Optimized Design of Compensation Capacitors for a Megahertz WPT System Using Full-Bridge Rectifier," in IEEE Transactions on Industrial Informatics, vol. 15, no. 1, pp. 95-104, Jan. 2019, DOI: 10.1109/TII.2018.2833209.

[5] M. Liu, M. Fu, Y. Wang and C. Ma, "Battery Cell Equalization via Megahertz Multiple-Receiver Wireless Power Transfer," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 4135-4144, May 2018, doi: 10.1109/TPEL.2017.2713407.

[6] M. Fu, H. Yin, and C. Ma, "Megahertz Multiple-Receiver Wireless Power Transfer Systems With Power Flow Management and Maximum Efficiency Point Tracking," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 11, pp. 4285-4293, Nov. 2017, doi: 10.1109/TMTT.2017.2689747.

[7] L. Jiang and D. Costinett, "A single-stage 6.78 MHz transmitter with the improved light load efficiency for wireless power transfer applications," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018, pp. 3160-3166, doi: 10.1109/APEC.2018.8341553.

[8] L. Jiang and D. Costinett, "A High-Efficiency GaN-Based Single-Stage 6.78 MHz Transmitter for Wireless Power Transfer Applications," in IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7677-7692, Aug. 2019, doi: 10.1109/TPEL.2018.2879958.

[9] Y. Shen, H. Wang, F. Blaabjerg, H. Zhao and T. Long : "Thermal Modeling and Design Optimization of PCB Vias and Pads", in IEEE Transactions on Power Electronics, vol. 35, no. 1, (2020)