High-Voltage Isolated Square Waveform Converter with DC-Offset Voltage for Physical Vapor Deposition (PVD) Applications

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***Abstract*— This paper proposes two isolated asymmetric rectangular waveform converters for high voltage pulse voltage generation from 100 V to -2 kV in surface coating by the physical vapor deposition (PVD) method. The PVD method is a surface coating method using chemical reactions of materials such as argon gas. The surface shape of the target sample is regulated by the external square waveform converter, which requires the capability of variable duty control and variable amplitude operation in order to manage the coating performance. This paper presents details of a circuit configuration that enables variable duty control from 0 - 100% and variable amplitude operation to 100 V. Furthermore, the load model in the PVD method is also shown to clarify the behavior of the square waveform converter. The experimental results show that the switching duty is variable by 50%, 20% and 80% with the positive voltage amplitude adjusted by 25% of the peak voltage.**

Keywords*— Isolated square waveform converter, Thin film coating equipment, PVD method, High voltage pulse generation.

I. INTRODUCTION

A thin film coating technology has been widely used to improve the wear resistance of metal components, such as cutting tools. The coating method is classified into two categories: chemical vapor deposition (CVD) and physical vapor deposition (PVD) methods. The CVD method is characterized by a high deposition rate, limited gas variety, and high temperatures in the deposition process. On the other hand, the PVD method is widely used because of attractive advantages, e.g., 1) variety of thin-film materials, 2) low-temperature deposition, and 3) high thin-film adhesion. The PVD method requires the external bipolar voltage source during the surface coating process in order to adsorb the coating material to the target sample [1]-[2]. This voltage source requires square waves of asymmetrical high-voltage, pulse width adjustment an operating frequency of 300 kHz or higher.

The conventional circuit provides asymmetrical high-voltage square waves by connecting two converters with different output voltage polarities. However, this circuit requires two DC input voltages of several kilovolts and several hundred volts. Besides, the conventional circuits require the switching devices with high-withstand voltages operating at several kilovolts. In [3], a boost inverter-based bipolar high-voltage converter is proposed in order to reduce the voltage applied to switching devices. The proposed converter is configured with two bidirectional DC-DC boost converters. The converter has a boost function by charge and discharge of two inductors to generate high-voltage bipolar output pulses from a low input DC voltage. However, a high withstand voltage is required for two of the four switching devices used in this converter. Furthermore, the output bipolar voltage is limited to a 50% duty cycle.

A bipolar pulse generator based on a Marx generator is proposed in order to control the pulse width with several switching devices and capacitors [4]-[6]. The Marx generator outputs a bipolar voltage with an H-bridge circuit connected in series on the load side. Furthermore, this circuit generates bipolar voltage without the need for an H-bridge by using a double power charging Marx generator or a cascade of positive and negative Marx generators. However, this circuit is a high cost because it requires a large number of high-withstand voltage components.

A half-bridge modular multilevel converter (HB-MMC) is proposed in order to reduce the voltage per switching device [7]-[12]. The HB-MMC arm is configured with several half-bridge sub-modules connected in series. The half-bridge submodule is configured with two switching devices and a capacitor. This topology is composed of two arms that charge the capacitors in parallel. The bipolar voltage is generated by controlling the discharge sequence. Furthermore, the duty cycle of the output bipolar voltage is varied by setting the switching sequence of each arm. However, the HB-MMC requires more complex control in order to maintain a balanced voltage across the capacitors.

This paper proposes an isolated asymmetrical square waveform converter configured with the two isolated converters to achieve voltage control, pulse width control, high switching frequency, and low input voltage. The originality of this paper is that the high-withstand switching device is not needed on the output side because the square wave voltage is boosted by the transformer. Furthermore, the proposed converter achieves variable duty cycle control and output voltage amplitude adjustment by combining the pulse generator circuit and a DC offset circuit. Experimental results from a prototype outputting a pulse voltage range of 25 V to

minas several hundred voltages demonstrated variable duty cycle control and amplitude adjustment functions.

This paper is organized as follows. Section II introduces the circuit configuration of the square waveform converter and basic operation waveform. Section III describes the control method of the proposed circuit. Section IV explains the load estimation method of the coating equipment. Section V presents experimental results to verify the validity of the proposed circuit.

II. Circuit Configuration

Fig. 1 shows the circuit configuration of the proposed square waveform converter. This circuit is configured with a pulse generator circuit and a DC offset circuit. The pulse generator circuit provides the high-frequency square wave voltage with an amplitude from 0 V to -2 kV. The transformer of the pulse generator circuit has a three-winding configuration with one input and two outputs. The input voltage v_{Lm1} of the three-winding transformer is a square wave voltage with only AC components after the DC component has been blocked by the blocking capacitor C_{blk}. The output voltage v_{Lm2} of the three-winding transformer is rectified to a DC voltage by diode D_{r1} and smooth capacitor C_{s1}. The output voltage v_{Lm3} of the three-winding transformer is an AC voltage with the primary transformer L_{m1} voltage as higher by the turn ratio. The pulse generator output voltage v_{sq} is the sum of v_{Lm2} and v_{Lm3}. The DC offset circuit provides DC voltage with a maximum voltage of 100 V. Furthermore, the power flow in the DC offset circuit changes depending on the polarity of v_{sq}. As v_{sq} outputs a positive voltage, a current flows through the load because the capacitor C_3 discharges electric charge. As v_{sq} outputs a negative voltage, a current flows to the input side through diode D_{r2} when the capacitor C_3 stores an electric charge. Thus, asymmetric square wave voltages are applied to the load from a maximum pulse voltage of 100 V to -2 kV. Besides, the diode clamp snubber circuit is applied on the secondary side in order to avoid resonance between the wiring inductance and the load capacitance component.

Fig. 2 shows the switching pattern of the pulse generator circuit at a 50% duty cycle. The pulse generator circuit operates in two operating modes. In mode I, the DC voltage of the load is supplied from the DC offset circuit. The full-bridge inverter circuit applies a positive voltage to the primary side of the transformer. In this case, the current flows in different directions in the two windings on the output side of transformer $T_{r.1}$. Therefore, the output transformer secondary voltage v_{sq} is 0 V because the transformer secondary voltages of v_{Lm2} and v_{Lm3} are canceled out. The DC voltage of the DC offset circuit is applied to the load because the pulse generator circuit and the DC offset circuit are connected in series. In mode II, A negative voltage is applied to the transformer primary side by a full-bridge inverter, which applied a negative voltage of several kilovolts peak to the load. The winding L_{m2} on the output side of the transformer $T_{r.1}$ does not output voltage because a reverse bias is applied to the rectifier diode D_{r1}. The output voltage is the sum of the smoothing capacitor voltage v_{Cs1} of the rectifier circuit and the secondary transformer output voltage v_{Lm3}.

Fig. 3 shows the switching pattern of the DC offset circuit at a 50% duty cycle. The DC offset circuit operates in two modes, as the pulse generator circuit. In mode I in Fig. 3, the current i_{L1} of inductor L_1 increases linearly because half of the DC voltage is output on the secondary side of transformer $T_{r.2}$.

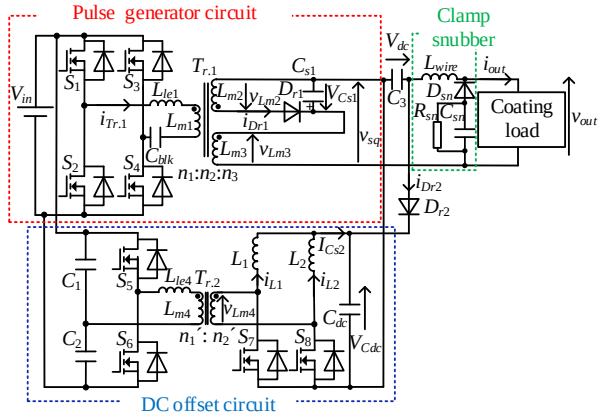


Fig. 1 Circuit configuration of proposed square waveform converter.

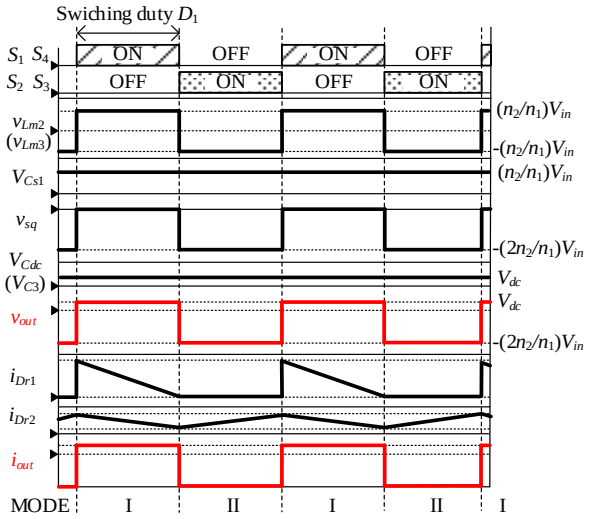


Fig. 2 Switching waveforms during square wave voltage output for pulse generator.

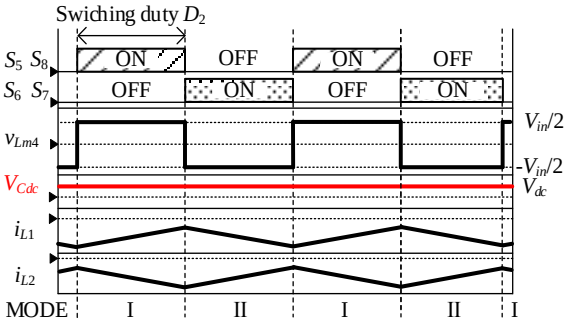


Fig. 3 Switching waveforms during DC offset voltage output for DC offset circuit.

In mode II of Fig. 3, the current i_{L2} of inductor L_2 increases linearly because negative voltage is output on the secondary side of transformer $T_{r.2}$. As a result, the output current I_{Cs2} of the DC offset circuit is twice the value of the inductor currents i_{L1} and i_{L2}. Thus, the output voltage V_{Cs2} is half the rms value V_{in} / 2 for the secondary voltage v_{Lm4} of transformer $T_{r.2}$.

III. Control Method of the Proposed Circuit

Fig. 4 shows the control block diagram of the proposed circuit. The two isolated converters each operate in an open-loop control. The pulse width of the square wave is controlled from 0% to 100% by varying D_1 from 0 to 1.0. The switching duty D_2 varies the duty cycle from S_5 to S_8 of the DC offset

circuit. The switching duty D_2 is required in order to vary the DC voltage at the output voltage V_{dc} of the DC offset circuit in the range of 0 to 100 V.

Fig. 5 shows the switching pattern when the duty cycle D_1 of the pulse generator circuit is varied. The secondary transformer output voltage v_{Lm2} has a voltage waveform with AC components only, because the DC components are cut off by the blocking capacitor C_{blk}. The relationship between the DC voltage V_{blk} of C_{blk} and the duty cycle D_1 is expressed as

$$V_{blk} = \frac{n_2 V_{in}(1-2D_1)}{n_1} \quad \text{.....(1)},$$

where V_{in} is the input voltage, n_1 is the number of primary turns of transformer $T_{r.1}$ and n_2 is the number of secondary turns of transformer $T_{r.1}$.

Fig. 5(a) shows the voltage waveforms when the duty cycle D_1 is less than 50%. In this case, the average AC voltage V_{acavg} increases in the positive direction at the secondary output voltage v_{Lm2} of transformer $T_{r.1}$. Furthermore, the DC voltage V_{blk} is added to the peak voltage V_{acpeak} and the bottom voltage V_{acbot} at v_{Lm2}. Fig. 5(b) shows the voltage waveforms when the duty cycle D_1 exceeds 50%. In this case, the average AC voltage V_{acavg} increases in the negative direction at the secondary output voltage v_{Lm2} of transformer $T_{r.1.}$ Furthermore, the DC voltage V_{blk} reduces the peak voltage V_{acpeak} and the bottom voltage V_{acbot} in v_{Lm2}. Moreover, the capacitor voltage V_{Cs1} after half-wave rectification of v_{Lm2} is added to the secondary voltage v_{Lm3} of the transformer $T_{r.1}$. As a result, the voltage amplitude $V_{p\text{-}p}$ has a negative voltage range below 0 V. Therefore, the termination voltage v_{sq} of the pulse generator circuit outputs a high-voltage pulse with a wide duty cycle range.

Fig. 6 shows the switching pattern when the duty cycle D_2 of the DC offset circuit is less than 50%. The average value of the AC voltage V_{acavg} increases in the positive direction because the voltage-time product relationship changes depending on duty cycle D_2 in the half-bridge inverter on the primary side of transformer $T_{r.2}$. Therefore, the relationship between the voltage division ratio of the capacitor voltages V_{C1} and V_{C2}, and the current ratio of the inductor currents i_{L1} and i_{L2} changes depending on the duty cycle D_2. The relationship between the DC output voltage V_{dc} and duty cycle D_2 is expressed as

$$V_{dc} = D_2(1-D_2)V_{in} \quad \text{.....(2)},$$

where D_2 is the duty cycle of the DC offset circuit.

Fig. 7 shows the principle of operation of an RCD clamp snubber [13]. The RCD clamp snubber suppresses resonance caused by the capacitive component of the load and the inductance of the wiring. The snubber capacitor C_{sn} absorbs the ringing energy in the load voltage. The snubber resistor R_{sn} consumes the energy charged in C_{sn}. The snubber resistor R_{sn} is calculated from the relationship between the discharge loss of C_{sn} and the resonance bottom of the load voltage $V_{\text{out\_min}}$ expressed as

$$R_{sn} = \frac{(V_{out\_\min})^2}{P_{Rs}} \quad \text{.....(3)},$$

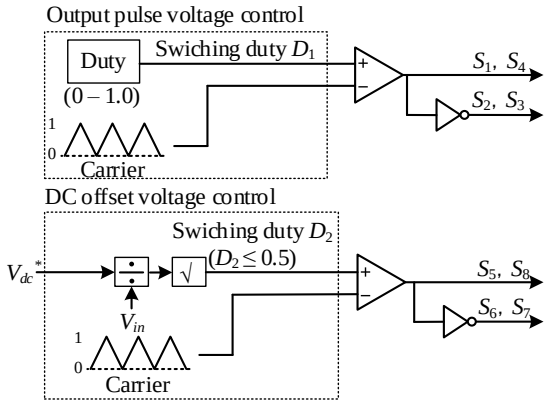
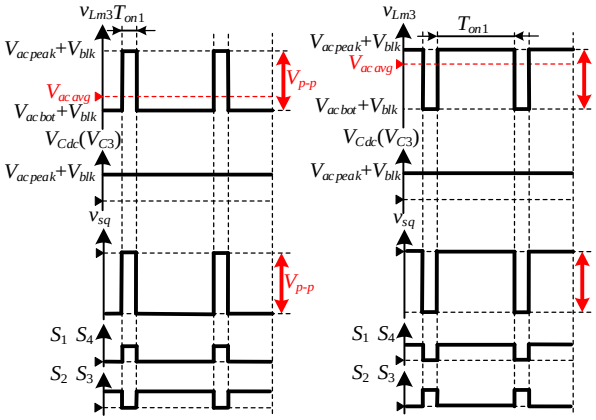


Fig. 4 Control block diagram of proposed square waveform converter.



(a) Duty D_1 < 50% (b) Duty D_1 > 50%

Fig. 5 Switching patterns of pulse generator circuit with variable Duty.

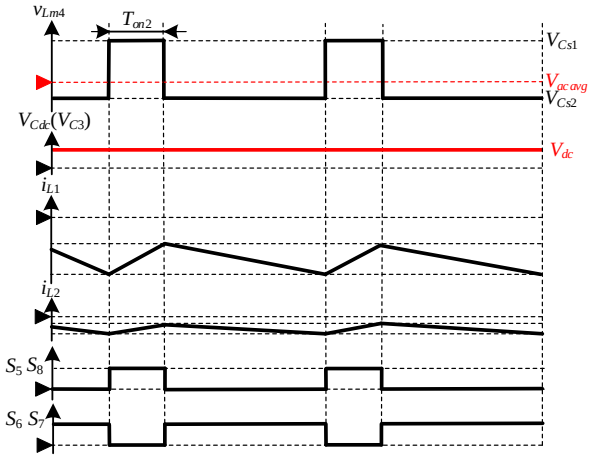


Fig. 6 Switching patterns of DC offset circuit with variable Duty (Duty<50%).

where V_{out_min} is the resonance bottom value of the load voltage, and P_{Rs} is the power dissipation in the snubber resistor.

The snubber capacitor C_{sn} is calculated from the relationship between R_{sn} and the switching period. it is expressed as

$$C_{sn} \gg \frac{T_{sw1}}{R_{sn}} \quad \text{.....(4)},$$

where T_{sw1} is the switching period of the pulse generator circuit.

IV. PARAMETER ESTIMATION OF COATING LOAD MODEL

A. Equivalent circuit model and parameter identification method

The proposed circuit is required to output a high-frequency bipolar voltage without ringing during transient states. However, the coating equipment behavior is unclear because of its non-linear characteristics. Thus, it is necessary to clarify the load model in order to analyze the operation of the proposed circuit. This chapter estimates the load parameters of the coating equipment using experimental waveforms.

Fig. 8 shows the operating waveforms of the coating equipment applying the proposed circuit. The coating load is analyzed from five operation modes.

In mode I, the load voltage v_{out} rises before S_1 is turned on because the energy stored in the leakage inductance Lle4 is discharged by the flow of negative current. In mode II, the load voltage rises sharply to a positive voltage as the load current direction becomes positive because capacitor C_{s1} discharges its electric charge through the freewheeling diodes of switches S_1 and S_4. Thus, the load voltage v_{out} in this mode becomes a positive voltage because the power is regenerated from the secondary side to the primary side of transformer $T_{r.1}$. In mode III, the load current waveform transiently rises as current flows through the RLC series circuit caused by transformer leakage inductance, load resistance components, and smoothing capacitors. In mode IV, the load current drops sharply in the negative direction while the load voltage drops slightly from its peak value V_{peak} because of the energy stored in the leakage inductance is discharged during the dead time T_{dead}. In mode V, the load voltage v_{out} and the load current iout are resonant due to the leakage inductance, the wiring inductance, and the capacitive component of the coating equipment.

Fig. 9 is the equivalent circuit of the coating equipment based on Fig. 8 in the state of plasma generation during the surface coating of the target sample. The equivalent circuit becomes an RLC circuit including the leakage inductance L_{le}, the wiring inductance L_{wire}, and the smoothing capacitor C_{s1}. The equivalent circuit for the plasma-generated state behaves as the positive charge layer (ion sheath) characteristics inside the equipment for diodes D_{out1} and D_{out2}. According to Fig. 9, the current flows in the RLC series circuit with R_{out1}, L_{le}, L_{wire} and C_{s1} when a positive voltage is applied. In mode III in Fig. 8, R_{out1} is calculated by the time constants of R_{out1} and Lle and L_{wire} expressed as

$$R_{out1} = \frac{(L_{le} + L_{wire})}{\tau} \quad \text{.....(5),}$$

where R_{out1} is the resistance component when a positive voltage is applied, and τ is the time constant of the series circuit of R_{out1}, L_{le}, and L_{wire}. According to Fig. 9, the current flows through the RC circuit in parallel with the L in series when a negative voltage is applied. In mode V of Fig.8, L_{le}, L_{wire}, and the load capacitance component C_{out} resonate. Thus, C_{out} is expressed from the resonance frequency expression as

$$C_{out} = \frac{1}{4\pi^2 f_{rin}{}^2 (L_{le} + L_{wire})} \quad \text{.....(6),}$$

where f_{rin} is the resonance frequency of L_{le}, L_{wire}, and C_{out}.

The resistance component R_{out2} when a negative voltage is applied is expressed by (7) from the relationship between the transfer function of the circuit by L in series and RC in parallel.

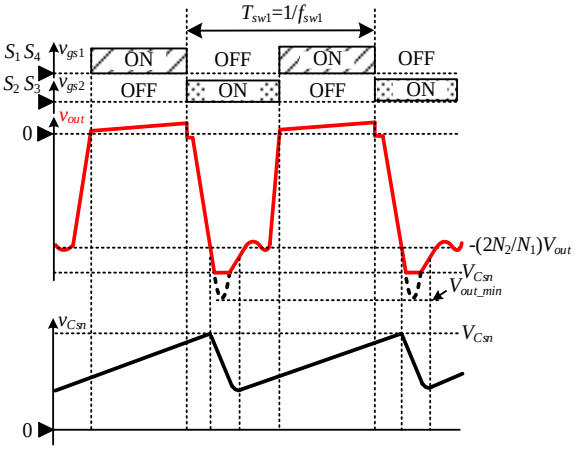


Fig. 7 Operating Principle of RCD clamp snubber during switching.

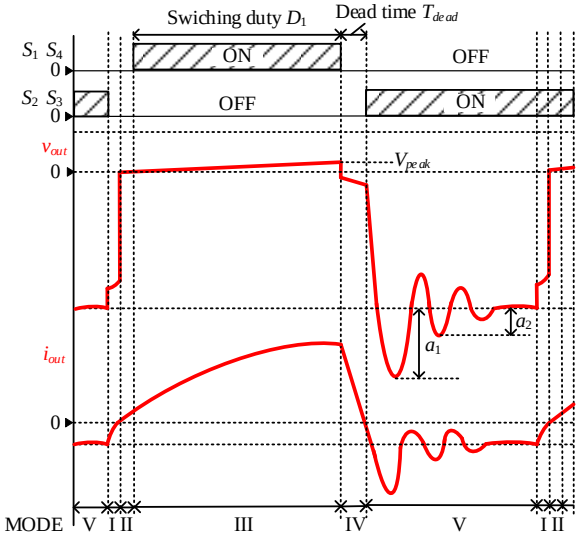


Fig. 8 Switching pattern when the proposed circuit is applied to the coating load.

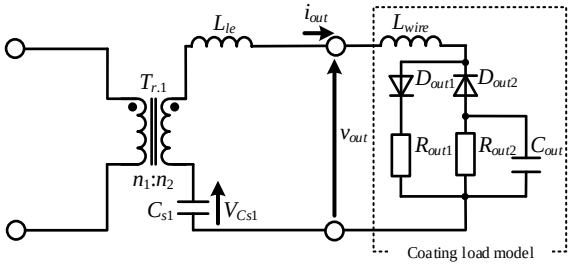


Fig. 9 Equivalent circuit model for coating load with square wave voltage applied.

$$R_{out2} = \frac{1}{2\zeta}\sqrt{\frac{(L_{le} + L_{wire})}{C_{out}}} \quad \text{.....(7),}$$

The damping coefficient ζ is expressed as

$$\zeta = \frac{\ln(a_1 / a_2)}{\sqrt{4\pi^2 + \{\ln(a_1 / a_2)\}^2}} \quad \text{.....(8),}$$

where a_1 is the resonance bottom value of v_{out} in mode V of Fig.8, and a_2 is the second resonance bottom value of v_{out} in mode V of Fig.8.

TABLE I. ELEMENT PARAMETERS USED FOR IDENTIFICATION OF COATING LOAD PARAMETERS

Element	Symbol	Value
Input voltage	V_{in}	40 V
Number of winding turns	n_1:n_2:n_3	6:10:10
Switching Frequency (Pulse generator circuit)	f_{sw1}	50 kHz
Resonance frequency	f_{rin}	833 kHz
Time constant	τ	6.30 µs
Leakage inductor (Pulse generator circuit)	L_{le}	6.52 µH
Wiring inductance	L_{wire}	1.00 µF
Resistance component (Positive pulse voltage applied)	R_{out1}	1.19 Ω
Capacitance component	C_{out}	4.85 nF
Resistance component (nagative pulse voltage applied)	R_{out2}	54.7 Ω

B. Parameter Identification Result

Table I shows the parameters in the simulation using the load model. The simulation parameters shown in Table I are set to low-voltage and low-frequency conditions to equal the experimental parameters in the coating load.

Fig. 10 shows the operating waveforms compared to the experimental and simulation results. According to the turn-off timing in Fig. 10., the load voltage V_{out} resonates due to the transformer leakage inductance L_{le}, the wiring inductance L_{wire}, and the load capacitance component C_{out} because the resistance component R_{out2} is small, which has little damping effect on the LC resonance. The load voltage v_{out} at turn-on timing shown in Fig. 10 does not resonate because the current does not flow through the capacitive component C_{out} of the load as shown in Fig. 9. Table II shows the results of comparing the operating waveforms for ringing amplitude and period. The load voltage waveforms in Table II show that the ringing amplitude ΔV has an error of 7.62% and the ringing period Δt_1 has an error of 8.21%, which are within 10% of each other. Furthermore, the load current waveforms in Table II show that the error in the ringing amplitude ΔI is 7.96% and the error in the ringing period Δt_2 is 1.34%, which are within 10% of each other. Thus, (5)-(8) applied to the parameter identification are valid.

V. EXPERIMENTAL RESULTS

Table III shows the experimental conditions for the proposed circuit. The switching frequency of the pulse generator circuit is set to 300 kHz, which is required for the coating equipment. The number of winding turns of the three-winding transformer is set to n_1:3 turns, n_2:8 turns, and n_3:8 turns respectively to output a negative voltage of 2 kV at 400 V input voltage. The basic operation of the proposed circuit is verified using a resistance load. Note that the RCD clamp snubber circuit is not applied because the experimental load is an inductive load that does not resonate.

Fig.11 shows the operating waveforms when the duty cycle D_1 of the primary side H-bridge of the pulse generator circuit is set to 50%, 20%, and 80%. Fig. 11(a) shows the asymmetrical square wave voltage at a switching duty D_1 of 0.5. The DC offset voltage of output voltage V_{Cs2} is set to 25 V. This corresponds to the DC voltage V_{dc} calculated by substituting the experimental conditions of an input voltage of 100 V and a duty cycle D_2 of 0.5 into (2). The ringing occurs during the transient phenomenon of the load voltage. The ringing of the load voltage occurs from resonance caused

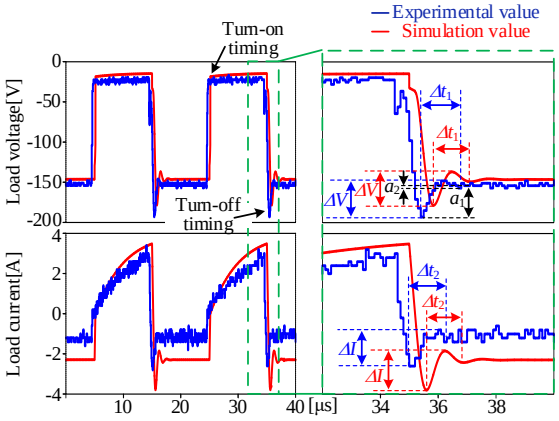


Fig. 10 Comparison of experimental results with coating load and simulation results with the equivalent circuit model.

TABLE II. COMPARISON OF ERROR RATES BETWEEN EXPERIMENTAL RESULTS AND EQUIVALENT CIRCUIT MODEL SIMULATION RESULTS

Name	Synbol	Experimental value	Simulation value	Error rate
Load Voltage ringing amplitude	ΔV	45.0 V	41.5 V	7.62%
Load voltage ringing cycle	Δt_1	1.30 µs	1.28 µs	8.21%
Load current ringing amplitude	ΔI	1.80 A	1.94 A	7.96%
Load current ringing cycle	Δt_2	1.30 µs	1.28 µs	1.34 %

TABLE III. EXPERIMENTAL PARAMETERS WITH RESISTIVE LOADS OF THE PROPOSED CIRCUIT PROTOTYPE

Element	Symbol	Value
Input voltage	V_{in}	100 V
Swiching frequency (Pulse generator circuit)	f_{sw_sq}	300 kHz
Swiching frequency (DC offset circuit)	f_{sw_dc}	100 kHz
Dead time	T_{dead}	100 ns
Number of winding turns (Pulse generator circuit)	n_1:n_2:n_3	3:8:8
Magnetizing inductor (Pulse generator circuit)	L_{m1}	278 µH
Leakage inductor (Pulse generator circuit)	L_{le1}	1.47 µH
Number of winding turns (DC offset circuit)	n_1´:n_2´	13.5:13.5
Magnetizing inductor (DC offset circuit)	L_{m2}	875 µH
Leakage inductor (DC offset circuit)	L_{le2}	2.19 µH
Boost inductor	L_1, L_2	100 µH
DC capacitor	C_1, C_2	50 µF
Output side capacitor	C_3	20 µF
Blocking capacitor	C_{blk}	25 µF
Load resistance	R_{out}	200 Ω

by the leakage inductance and stray capacitance in the three-winding transformer. The resonant frequency of the ringing agrees with the resonant frequency of the three-winding transformer due to its leakage inductance of 2.22 µH and stray capacitance of 183 pF. Fig.11(b) shows the asymmetrical square wave voltage at a switching duty D_1 of 0.2. As shown in Fig.11(b), the ringing of the load voltage occurs due to resonance caused by the leakage inductance and stray capacitance of the three-winding transformers, the same as in Fig.11(a). However, the load voltage v_{out} shown in Fig. 11(b) has a larger resonance amplitude at turn-on or turn-off than in Fig. 11(a) because the current rises sharply as the turn-on period becomes short. Fig.11(c) shows the asymmetrical

square wave voltage at a switching duty D_1 of 0.8. As shown in Fig.11(c), the resonance effect is small due to leakage inductance and stray capacitance because of the slow rise in current caused by the long turn-on period.

Fig. 12 shows the operating waveforms when the duty D_2 of the switches S_5-S_8 in the DC offset circuit is changed to 10%. Fig. 12. shows that setting D_2 of 0.1 results in a V_{dc} of 10 V. The V_{dc} value of 9.0 V calculated by substituting the experimental conditions into (2) agrees with the measured value within an error of about 10%. Comparing the load voltage V_{out} in Fig. 11(a) and Fig. 12, the effectiveness of the variable amplitude function was confirmed as the positive pulse voltage amplitude reduced from 25 V to 10 V.

VI. CONCLUSION

This paper proposed an isolated square waveform converter for PVD applications. The proposed circuit achieves variable duty and pulses positive voltage amplitude adjustment functions by combining two isolated converters. In addition, the load model parameters were identified in order to clarify the nonlinear load behavior. As a result of parameter identification, the amplitude and period of the ringing generated in the load voltage and load current were agreed within an error of 10%. The experimental results show that the adjustment functions of the pulse width and offset voltage of the asymmetrical square wave voltages are obtained by changing switching duty D_1 and D_2, respectively. Future work includes verifying operation when a PVD application is connected as a load.

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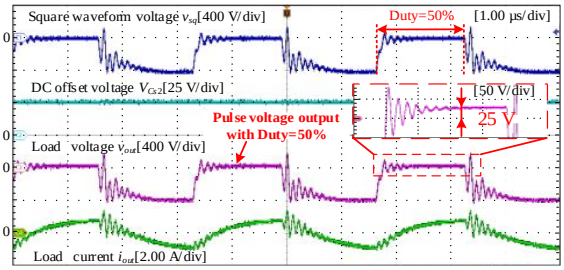
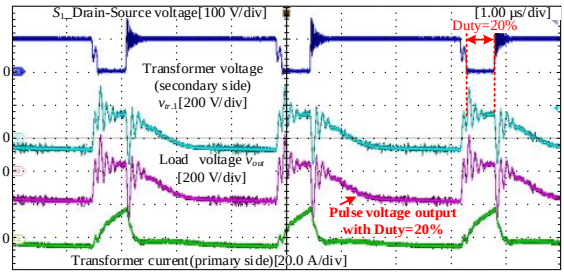
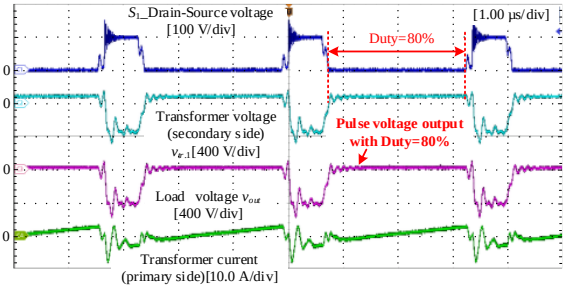


(a) Operating waveform of the proposed circuit.
V_{in} = 100 V, R_{out}=200 Ω, D_1=50%, D_2 = 50%

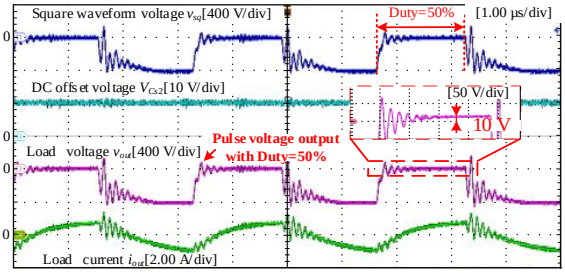


(b) Operating waveform of the proposed circuit.
V_{in} = 100 V, R_{out}=200 Ω, D_1=20%, D_2 = 50%



(c) Operating waveform of the proposed circuit.
V_{in} = 100 V, R_{out}=200 Ω, D_1=80%, D_2 = 50%

Fig. 11 Operating waveform for variable duty control.



V_{in} = 100 V, R_{out}=200 Ω, D_1=50%, D_2 = 10%

Fig. 12 Operating waveform for variable amplitude control.

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