Key Technologies for High-Efficiency and Reliable Solid-State Transformers for DC Microgrids

Keita Ohata
Naoto Kikuchi
Hiroki Watanabe
Keisuke Kusaka
Yushi Miura
Jun-ichi Itoh
Department of Electrical, Electronics
and Information Engineering,
Nagaoka University of Technology
Nagaoka, Japan
keita_ohata@stn.nagaokaut.ac.jp
n_kikuchi@stn.nagaokaut.ac.jp
hwatanabe@vos.nagaokaut.ac.jp
kusaka@vos.nagaokaut.ac.jp
miurayushi@vos.nagaokaut.ac.jp
itoh@vos.nagaokaut.ac.jp

Shota Urushibata
Meidensha Corporation
Numazu, Japan
urushibata-s@mb.meidensha.co.jp

Shinichiro Nagai
Pony Electric Co., Ltd
Yokohama, Japan
s-nagai@pony-e.jp

Tsuyoshi Funaki
Division of Electrical, Electronic
and Infocommunications Engineering,
Osaka University
Osaka, Japan
funaki@eei.eng.osaka-u.ac.jp

***Abstract*— This paper introduces key technologies for improved reliability of practical solid-state transformers (SST) to enable massive expansion of renewable energy. SSTs are attractive as compact and high-efficient AC-DC converters because SSTs accept a direct connection from medium voltage AC grid to DC microgrids without line-frequency transformers (LFTs). However, SSTs have low reliability compared with conventional AC-DC converters using LFTs. This paper introduces our contributions to the implementation of SSTs in society as follows: 1) conducted noise reduction by modulation technique, 2) cell-fault tolerant control, 3) packaging technology of power module for enhanced isolation and noise reduction, 4) development of high-frequency transformer with high voltage tolerance and 5) integrated system design for a 1-MVA SST towards practical operation.**

Keywords— solid-state transformer; renewable energy; DC grid

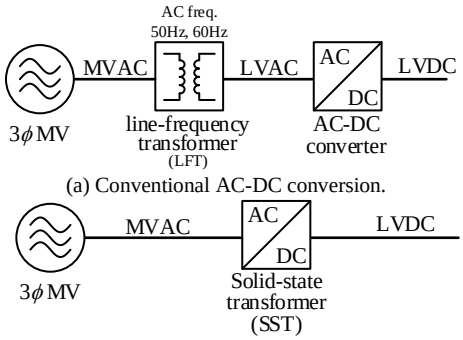
I. INTRODUCTION

Currently, the mass introduction of renewable energy, such as solar and wind power and electric vehicles (EVs), is progressing toward the realization of carbon neutrality. However, renewable energy is unfortunately recognized as an unstable power supply because the generating power of renewable energies depends on the natural environment. In addition, a fluctuation of power consumption by EV chargers is uncertain. As a solution to this problem, a low-voltage DC microgrid installation is a suitable option for direct coupling between variable power demand and renewable energy.

Fig. 1 shows the comparison of AC grid to DC grid interfaces between conventional interfaces containing a line-frequency transformer (LFT), and a solid-state transformer (SST). SSTs bring some advantages such as higher efficiency, smaller size, and lower cost because the number of power conversions is reduced compared with conventional AC grid–DC grid interfaces [1]. Thus, SST has been highlighted as an important technology for DC microgrids. However, the low-voltage DC distribution systems have not been spread because of their low reliability compared with conventional AC-DC interfaces containing LFTs.

This paper describes key technologies for the development of a 1-MW SST with high efficiency and high power density, which maintains a stable power supply even with a large number of renewable energy sources. This development was carried out from five perspectives as follows:

A) conducted noise reduction by modulation scheme
B) short fault tolerant control utilizing phase-shift PWM with sawtooth carrier
C) packaging technology for enhanced isolation and noise reduction
D) development of 1-MVA 6.6-kV SST cell with high-voltage tolerance with a high-frequency transformer



(a) Conventional AC-DC conversion.

(b) AC-DC conversion using solid-state transformers.

Fig. 1. Comparison of AC grid-DC grid interfaces between conventional interfaces containing a line-frequency transformer (LFT), and a solid-state transformer (SST).

E) integrated system design for a 1-MVA SST towards practical operation

From these contributions, one of the guidelines for the practical SSTs has been identified.

II. Key Technologies to Improve Reliability of Practical SSTs

A. Gradational modulation for conducted noise reduction

Fig. 2 shows a photograph of a 13.5 kW, 27-cell prototype SST. Fig. 3 shows the configuration of the SST. This SST is a scaled-down power of the 1 MW SST, designed with a single-cell rating of 500 W. The SST consists of nine cells per phase, which are connected in series on the AC side and in parallel on the DC side. Each cell consists of a full bridge of power factor correction (PFC) converter and an LC resonant DC-DC converter.

Fig. 4 shows the output voltage of each cell. Typically, the basic modulation employs PWM output at all cells. In contrast, the proposed gradational modulation contains 1) PWM output in only one cell and 2) square-wave output synchronized with the grid voltage in other cells. As a result, the proposed modulation reduces conduction noise from the SST by suppressing common mode voltage fluctuations [2].

Fig. 5 shows the experimental results of the conducted emission from the developed 27-cell prototype SST. The proposed gradational modulation reduces the conducted emissions from the SST by 11dB in the 200 kHz band and 7dB in the 2 MHz band, respectively.

B. Fault-tolerant control utilizing phase-shift PWM with sawtooth carrier

A short fault-tolerant control utilizing phase-shift PWM with sawtooth carriers was developed for a cascaded modular converter [3]. The proposed fault-tolerant control is also applicable to open-circuit fault case by bypassing the AC-terminal of the failed sub-module (SM).

Fig. 6 shows a principle of the short-fault-tolerant control. This figure assumes a short circuit fault has occurred in a SM, and it has been identified. It is also assumed that SM operates

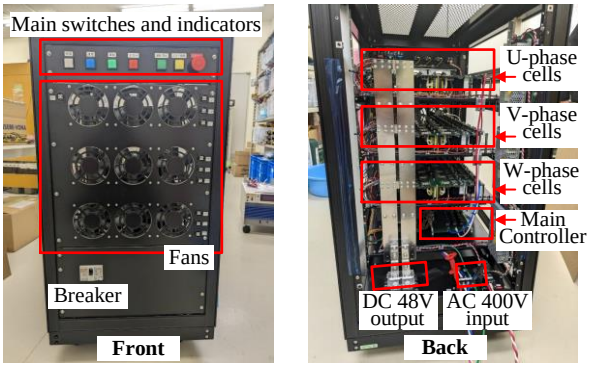


Fig. 2 Photographs of 27-cell SST (13.5 kW rated).

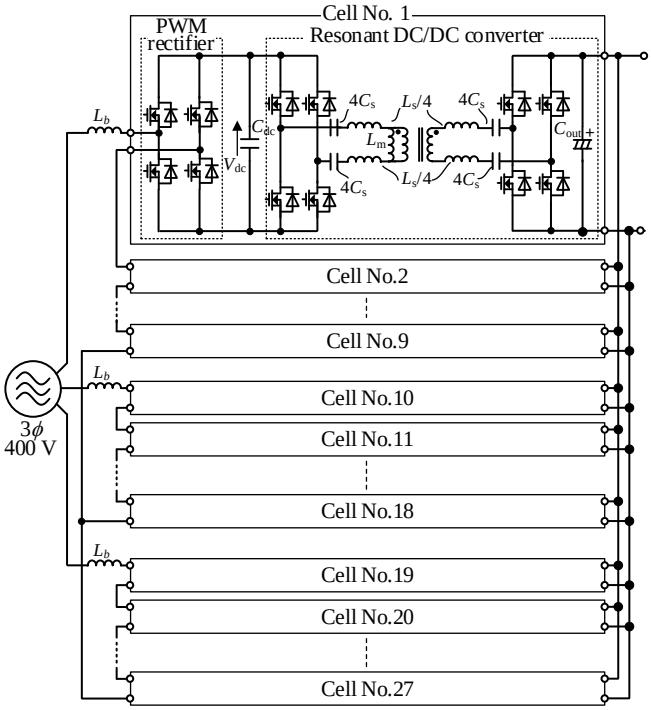
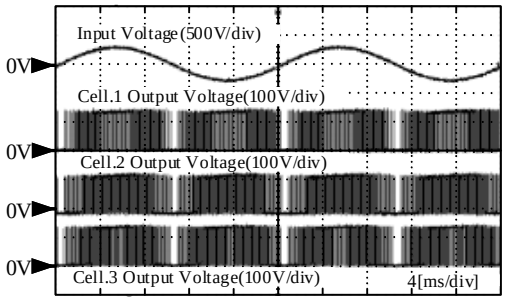


Fig.3 Prototype configuration of three-phase 27-cell SST.

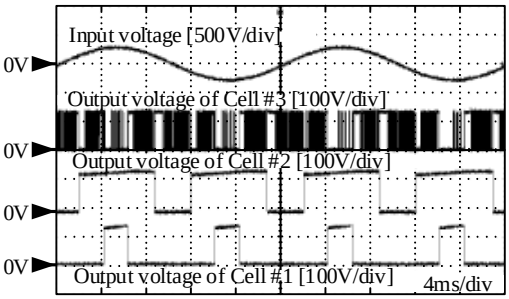
with unipolar modulation using sawtooth carriers, and further that the cascaded modular converter operates with a phase-shift PWM method. The figure assumes that two SMs are connected in each phase and that one SM fails to short-circuit in the U phase. The output voltage of a faulty SM is always zero because the output of a faulty SM is always short circuit. Thus, the output phase voltage of SST changes $\pm V_{dc}$ after a short fault. In addition, the output phase voltage is distorted.

Then, the developed fault-tolerant control adjusts the pulse patterns of other healthy SMs to maintain the line-to-line voltages. From Fig. 6, the U-phase-to-V-phase voltage is $2V_{dc}$ instead of the command value of 3 V_{dc} at the short fault. However, the fault-tolerant control recovers the line-to-line voltages.

Fig. 7 shows the output voltage vector in a U-phase SM fault, such as Fig. 6. At this time, the line-to-line voltage is maintained at 3 V_{dc} by reducing the output phase voltage by -V_{dc} using a submodule of the V phase and W phase, which is the healthy



(a) PWM switching in all cells (conventional modulation).



(b) proposed gradational modulation.

Fig. 4 Comparison of output voltage of each cell.

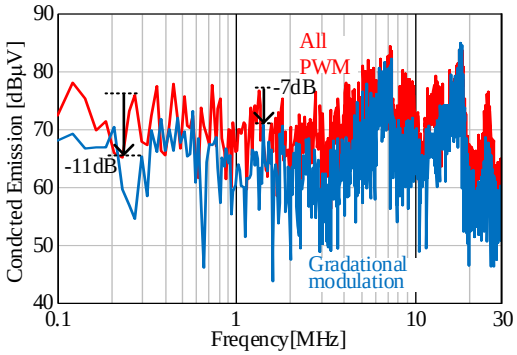
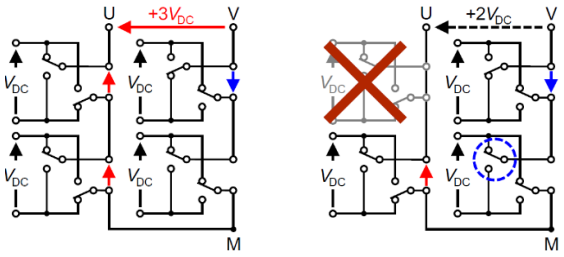


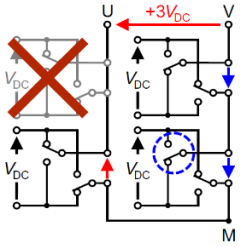
Fig. 5 Comparison of conducted emission from prototype SST.

phase. The notable features of the fault-tolerance control are: 1) additional switching is not required to adjust the pulse pattern because of the utilization of sawtooth carriers, and 2) redundant SM is not needed to operate the developed fault-tolerant control.

Fig. 8 shows the experimental result at short fault. The experiment assumes a short fault of one SM in the U phase and the W phase, respectively. The total harmonic distortion (THD) of line-to-line voltage increases from 13.2% to 17.8% by SM fault when the proposed tolerance control is not applied. In contrast, The THD improves from 17.8% to 13.7% which is equivalent to the THD before the SM fault when the proposed tolerance control is applied. However, the power imbalance among cascaded cells occurs by the proposed control. Then, the proposed fault-tolerance control also provides the power balance function. Thus, the SM load imbalance caused by the proposed control is suppressed by swapping the switching pattern between cascaded sub-modules.

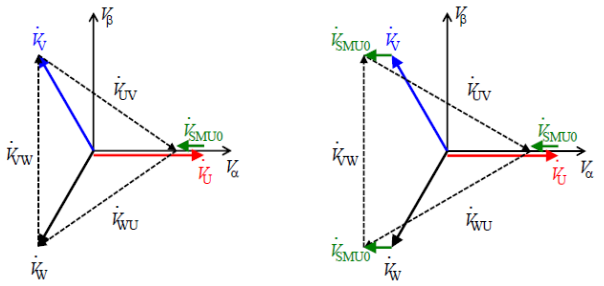


(a) Normal. (b) Fault occurs.



(c) Short-fault-tolerant control is applied.

Fig. 6 Principle of cell fault tolerant control.



(a) without the fault-tolerant control. (b) with the fault-tolerant control.

Fig. 7 Output voltage vector in case of SM U_0 is short fault.

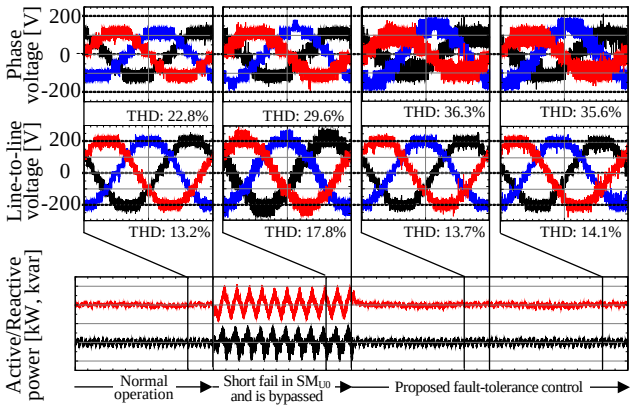


Fig. 8 Phase voltage and line-to-line voltage waveform when a short fault occurs in one SM of U-phase and V-phase, respectively.

C. Packaging technology of power module for enhanced isolation and noise reduction

This section describes low EMI noise and low thermal resistance power modules with high voltage tolerance.

1) Noise reduction:

Fig. 10 shows the drain-source voltage waveform, which is compared with the developed module and a commercial power module with a snubber circuit as shown in Fig. 9. In order to efficiently reduce surge voltage, minimizing ESL between a

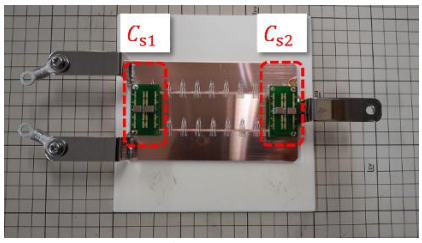
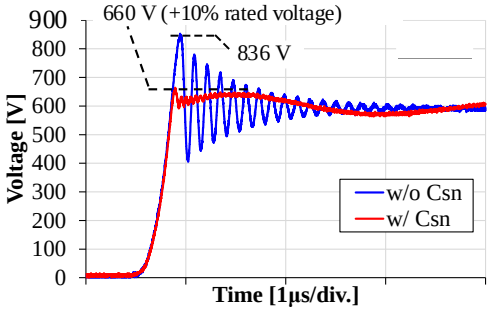
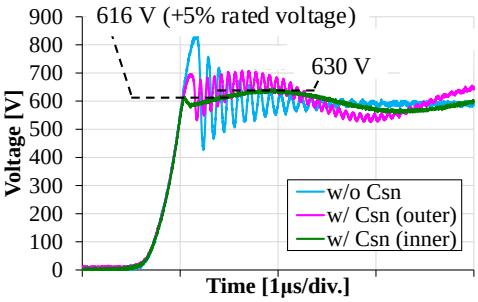


Fig. 9 Internal photograph of developed module with built-in snubber circuit.



(a) Commercial module (BSM600, Rohm).



(b) Developed module

Fig. 10 Switching waveform.

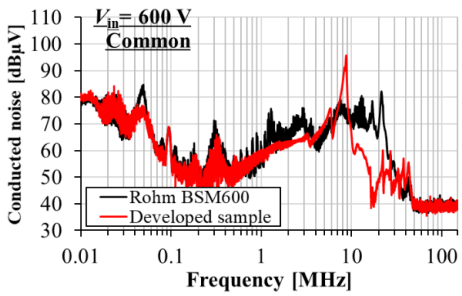


Fig. 11 Conducted noise spectrum.

snubber circuit and a switching device is effective. Thus, the snubber circuit embedded module is developed.

Fig. 11 shows the conducted noise from these power modules. The parasitic capacitance between the module wiring and the ground is only 264 pF. Thus, the conducted noise is reduced by up to 15dB compared with a commercial device at 100 kHz ~10 MHz band. In contrast, the conducted noise is increased at 8 MHz. The mechanism needs further investigation.

2) Improved cooling performance:

Placing power devices in close proximity reduces to parasitic inductance of power modules. Hence, a lower switching noise

Fig. 12 Photograph of developed power module.

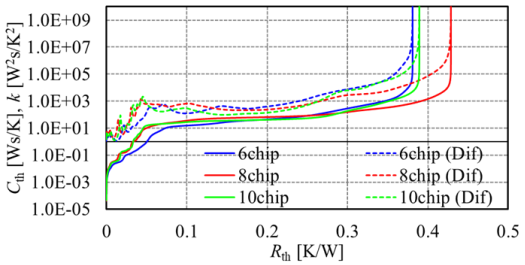


Fig. 13 Structure functions of developed power module.

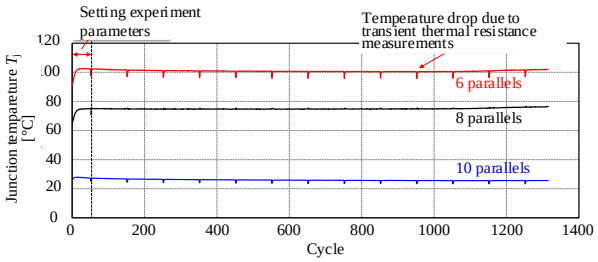


Fig. 14 Heat cycle test of developed module.

of the power module is achieved. In contrast, the cooling performance is decreased due to thermal interference between the power devices. From this perspective, the design was carried out with balancing while adjusting for thermal diffusion by the wiring layer conductor area and the parasitic inductance by the wiring path length. In addition, in order to mount MMC cells of different voltages on the same heat sink and to reduce the size of the SST, a module with a ground insulation voltage of 20 kV was designed.

Fig. 12 shows photographs of a developed power module which is designed for a rating of 600 V and 300 A.

Fig. 13 shows the structure functions of the developed power module, which are derived from a measured result of transient thermal resistance. The coordinate of origin is the junction of the power device. The horizontal axis shows the integrated thermal resistance from the chip, die-attach, copper wiring, insulating substrate, and heat sink as one moves to the right. The vertical axis shows the integrated heat capacity for each component. From this figure, the thermal resistance of the power module achieves 0.4 K/W. The conduction loss was only 198 W at maximum rated operating conditions. Thus, the power module enables continuous operation at an upper operating temperature of SiC-MOSFET (175°C).

Fig. 14 shows the heat cycle test of the developed module. the figure shows that even after 1000 cycles in the heat cycle test, no significant increase in junction temperature due to

degradation was observed. Thus, the developed power module has sufficient thermal cycle reliability.

D. Development of high-frequency transformer with high voltage tolerance

This section introduces a developed high-frequency transformer with a 6.6 kV voltage tolerance. An LFT for a 6.6 kV grid requires a large core to prevent magnetic saturation of the core. In contrast, SST employs a high-frequency transformer as a replacement for an LFT. Thus, the volume reduction of the transformer is achieved. However, high-frequency transformers used in SSTs need to maintain a high voltage tolerance between the primary windings and secondary windings. Thus, the clearance between the transformer windings and the core needs to be kept. Thus, downsizing high-frequency transformers is challenging. In this development, a prototype transformer that combines miniaturization with high voltage tolerance was developed using ferrite core and bobbin molding technology [4].

Fig. 15 shows a photograph of evaluated transformers. The developed bobbin-molded transformer was evaluated in comparison with unmolded and wiring-molded transformers.

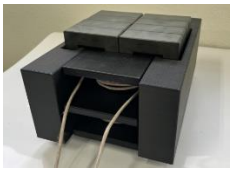
Fig. 16 shows the experimental results of partial discharge testing. This study defines a discharge start voltage as a voltage at which the amount of charge exceeds 50 pC. The partial discharge test results showed that the discharge start voltage of the transformer without mold is 2.66 kV, the winding-molded transformer is 9.67 kV, and the bobbin-molded transformer is 7.32 kV. The bobbin-molded transformer has significantly improved insulation performance compared to unmolded transformers. Moreover, the bobbin-molded transformer is verified to be applicable to SSTs for 6.6 kV systems. Unfortunately, the bobbin-molded transformer has inferior insulation performance compared to the winding-molded transformer. However, the proposed transformer has an advantage on cooling because it enables forced cooling around the windings.

E. Development of 1-MVA 6.6-kV SST cell

Table I lists the specifications of a cell that was developed for use in the 1-MVA SST. The developed cell is designed with a rated input voltage of 423 V, a rated input current of 87.5 A, a rated power of 37 kW, and a maximum efficiency of 98%. The circuit configuration is the same as in Fig. 3. The high-frequency transformer uses the transformer described in *Section D*.

Fig. 17 shows the operating waveform at the rated output power of 37 kW. The continuous operation has been verified under rated conditions.

Fig. 18 shows the efficiency of the developed cell. The maximum efficiency of 96.3% is achieved. The conversion efficiency is 1.7pt below the target efficiency of 98%. This is primarily due to the losses in the AC inductors. As the AC inductors are not optimally designed, further improvements in the overall system efficiency are expected. The volume of the developed cell is reduced by 62.5% compared to the conventional system that contains LFTs. Therefore, the developed 1-MVA SST is expected to achieve a 50% volume reduction compared to conventional systems.

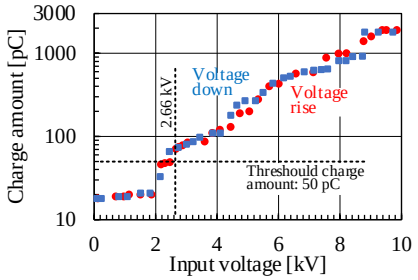


(a) Non-molding.

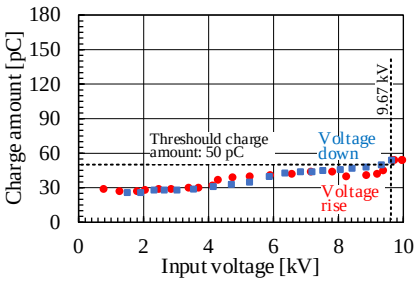
(b) Wiring molding.

(c) Bobbin molding (proposal).

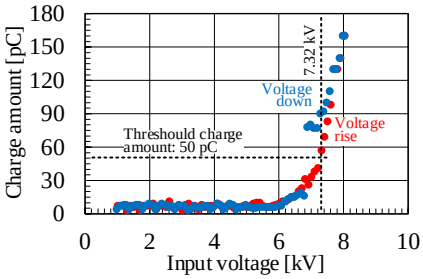
Fig. 15 Photograph of prototype transformers.



(a) Non-molding.



(b) Wiring molding.



(c) Bobbin molding (proposal).

Fig. 16 Experimental results of partial discharge testing.

F. Integrated system design for a 1-MVA SST towards practical operation

This section considers the volume and loss analysis of the development target of 1-MVA SST. In this section, DC-DC circuit topology employs a dual active bridge (DAB).

Table II lists the target specifications for the 1-MVA SST. The target specifications are based on 50% volume reduction and 60% weight reduction, compared with conventional systems with LFTs. In order to achieve these target

Table I. Design specifications of 37-kW prototype cell for 1-MW SST.

Item	Unit	Value			Remarks
		Min.	Typ.	Max.	
Input AC voltage	V_{rms}	384.9	423.4	442.6	
Input AC current	A_{rms}	83.7	87.5	96.2	
DC rated output power	kW		37		
DC output current	A		92.6		
AC input power	kW		37.8		Design efficiency: 98%
Input AC frequency	Hz		50/60±2%		
Input power factor			0.9		
Switching freq. at boost PFC conv.	kHz	10			
Switching freq. at res. DC-DC conv.	kHz	30			
Size	mm	1050 × 200×900			
Cooling		Forced air cooling			

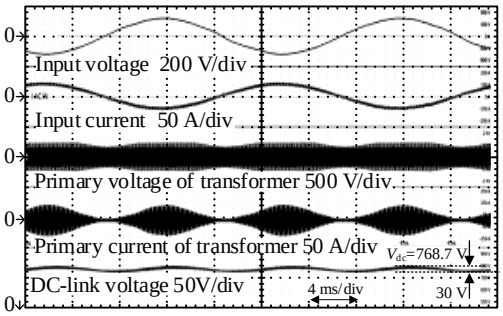


Fig. 17 Operating waveform of prototype cell for 1MW SST at rated power 37 kW.

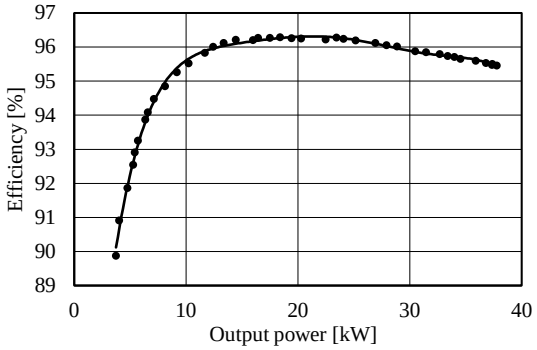


Fig. 18 Efficiency of 37-kW prototype cell.

specifications, an optimized design flow was established, which takes into account the design of the electrical components such as semiconductor modules, heat sinks, magnetic components and capacitors, and the layout.

Fig. 19 shows the simulation result of loss analysis. The efficiency of 99% is predicted under the simulated conditions. When the condition of the switching frequency is set to 50 kHz, and the external inductance is 5 μH, the iron loss increases. The reason is the iron loss of the employed core increases rapidly in the high-frequency range.

Fig. 20 shows the simulation result of volume-weight analysis. The volume and the weight are reduced as the switching frequency increases. However, in the 5 kHz~10 kHz range, the variation is small due to the large core and the small winding reduction with increasing switching frequency.

From this analysis, the cell of the developed 1MVA SST achieves an efficiency of 98%, a volume of 140 L, and a weight

Table II Target volume and weight of 1MVA SST (without control unit).

Volume Weight	≦ 6,870 L ≦ 3,372 kg
Input interface/filter	1,168 L (17% of entire system)
Cell	5,184 L (75% of entire system) ≦ 960 kg (29% weight of entire system)
Output interface	343 L (8% volume of entire system)

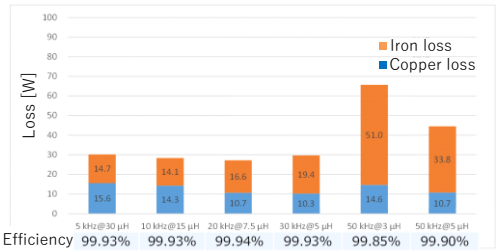


Fig. 19 Simulation result of loss analysis of 1 MVA SST.

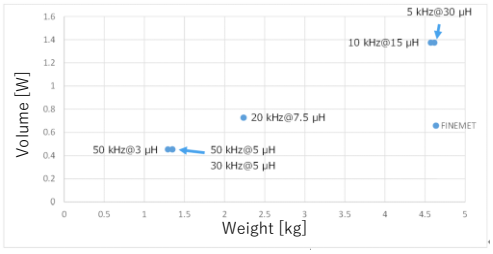


Fig. 20 Simulation result of volume-weight analysis of 1 MVA SST.

of 39 kg. The entire SST system is expected to achieve a volume of 3,366 L (49% of the target volume) and a weight of 994 kg (28% of the target weight).

III. Conclusion

This paper introduced key technologies for improving the reliability of practical SSTs to enable the massive expansion of renewable energy. These developed technologies identify the design guidelines for a 1 MW practical SST, which is connected directly between AC 6.6 kV and DC 400 V.

Acknowledgment

This paper is based on results obtained from a project, JPNP14004 subsidized by the New Energy and Industrial Technology Development Organization (NEDO).

References

[1] T. Dragičević, X. Lu, J. C. Vasquez and J. M. Guerrero, "DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues", IEEE Trans. Power Electron., vol. 31, no. 5, pp. 3528-3549, 2016

[2] N. Kikuchi, H. Watanabe, and J. Itoh, "Modeling of Common-Mode Noise Equivalent Circuit for Solid-State Transformer based on ISOP Configuration", EMC Japan/Asia-Pacific International Symposium on Electromagnetic Compatibility, pp.380-383, 2024

[3] Y. Aoki and Y. Miura, "Pulse Compensation for Phase-Shift PWM with Sawtooth Carrier Applied to Cascaded Multilevel Converter under Fault Condition", 2023 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 3569-3576, 2023

[4] R. Yonetomi, K. Kusaka, N. Koike, and S. Nagai, "Partial Discharge Test of High-frequency Transformers with Plastic Mold for SST", 2024 IEEE 10th International Power Electronics and Motion Control Conference, pp. 3007–3012, 2024