Clarification of Acceptable PWM Voltage Detection Delay for Current Source Type Electric Motor Emulator

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Abstract - This paper identifies acceptable voltage detection delay times to maintain the current response of the current source type electric motor emulator (EME). The EME has to detect the output voltage of an inverter under test (IUT). However, the detection delay when using a low-pass filter (LPF) for PWM voltage may decrease the accuracy of the EME. The acceptable delay time that maintains the desired current response is determined using Bode diagrams. As a result, in order to avoid affecting the IUT control, the LPF cutoff frequency should be selected eight times or higher than the IUT current control bandwidth.

Keywords: Motor drive system, Electric motor emulator (EME), Current control, low-pass filter (LPF)

I. Introduction

Electric motor emulator (EME) systems, which imitate various motor behaviors using a power converter, have been gaining attention in the development of adjustable speed drive systems, such as those used in electric vehicles (EVs)[1]. One of the most significant differences between an actual motor and an EME is that the PWM voltage of the output voltage of the inverter under test (IUT) must be detected. Therefore, the accuracy of the EME is affected by the detection of the output voltage of the IUT.

An LPF is a simple method for detecting the modulated voltage from the PWM voltage. However, the detection delay caused by the LPF poses a challenge in terms of stability and accuracy.

This paper clarifies the acceptable PWM voltage detection delay using an LPF in order to improve ease of implementation.

II. Current Source Type Electric Motor Emulator

Fig. 1 shows the inver test system using the current source type EME. The EME replicates the motor current according to the current command calculated by the motor model. In this paper, the state equation of the target motor is implemented as the motor model. The state equation of an interior permanent magnet synchronous motor (IPMSM) in the dq-axis is expressed as

$$
P\begin{bmatrix} i_a \\ i_a \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_a} & \omega_{\rm re} \frac{L_{\rm q}}{L_{\rm d}} \\ -\omega_{\rm re} \frac{L_{\rm d}}{L_{\rm q}} & -\frac{R}{L_{\rm q}} \end{bmatrix} \begin{bmatrix} i_a \\ i_a \end{bmatrix} + \begin{bmatrix} \frac{v_{\rm d}}{L_a} \\ \frac{v_{\rm q}}{L_{\rm q}} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{\omega_{\rm re} \psi_{\rm m}}{L_{\rm q}} \end{bmatrix} \dots (1),
$$

where i_d and i_q are the dq-axis current, v_d and v_q are the dqaxis voltage, R is the armature resistance, L_d and L_q are the dq-axis synchronous inductance, $\omega_{\rm re}$ is the electric angular frequency, ψ_m is the flux linkage of the permanent magnet, and *P* is the differential operator.

Fig. 1 Configuration of an inverter test system using an EME.

Here, the output torque T_{out} and the relationship between the electric angular frequency and the output torque on the dq-axis are expressed as

out ^m ^q ^d ^q ^d ^q *^T ^p ⁱ ^L ^L ⁱ ⁱ* ⁼ ⁺ [−] { () }(2),

re out ^L () *p P T T J* ⁼ [−] ...(3),

where T_L is the load torque, p is the pairs of poles, and J is the inertia of the motor.

The current commands are obtained by solving the differential equations (1), (2), and (3) using the backward Euler method in a DSP. The input of (1) is the output voltage of the IUT. In other words, the detected PWM voltage is used as the input of the state equation.

III. Analysis of Acceptable Voltage Detection Delay

Fig. 2 shows the analysis model based on the dq-axis. In this paper, field-oriented control (FOC) is implemented in the IUT controller, and the q-axis current command is calculated from the torque command. The d-axis current command is set to zero. Furthermore, decoupling control for the IPMSM dq-axis coupling term is implemented. The motor speed is fixed at 3600 r/min.

Fig. 3 shows the closed-loop Bode diagram of the inverter test system. Note that the current control bandwidth of both the IUT and the EME are set to 500 Hz and 2000 Hz. A gain

Fig. 2 Analysis model based on the dq axis of inverter test system using current source type electric motor emulator.

peak does not occur when the LPF cutoff frequency exceeds 3 kHz, which means the detection delay caused by the LPF is acceptable. In contrast, a gain peak occurs when the LPF cutoff frequency is 3 kHz or less. Thus, the LPF cutoff frequency should be selected eight times or higher than the IUT current control bandwidth. In addition, compensation should be applied when the delay caused by the LPF is unacceptable.

IV. Experimental Result

Fig. 4 shows the difference in the current response with and without an LPF with an acceptable detection delay time. In Case A, the modulated waveforms of the PWM are input directly from the IUT controller to the EME controller in order to verify the influence of the LPF. Without an LPF, no overshoot is observed in the q-axis current. Similarly, no overshoot is evident when the IUT output voltage is detected by an LPF with a cutoff frequency of 4 kHz. Therefore, the current response is equivalent to that without an LPF when an LPF has an acceptable PWM voltage detection delay time.

Fig. 5 shows the current response when an LPF with an unacceptable detection delay is used. Note that the cutoff frequency of the LPF is set to 1 kHz. The phase lead compensation is applied to compensate for the detection delay caused by an LPF. As shown in (a), an overshoot occurs in the q-axis current, and the phase current is distorted by an LPF with a 1 kHz cutoff frequency. In contrast, phase lead compensation suppresses the overshoot and prevents distortion of the phase currents, as shown in (b). Therefore, compensating for the unacceptable voltage detection delay maintains the desired current response even when an LPF with a low cutoff frequency is used.

References

[1] S. Hamada, T. Takahashi, N. Kezuka, M. Kouketsu and S. Ishigaki, "Inverter Drive of Dynamometers for Automotive Evaluation System," 2018 International Power Electronics Conference (IPEC-Niigata 2018 - ECCE Asia), Niigata, Japan, 2018, pp. 227-232.

Fig. 3 Closed loop Bode diagram for cutoff frequency variation.

