Active Power Decoupling Method based on Dual Active Bridge Converter without additional components

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Abstract— **This paper proposed an active power decoupling method using a Dual Active Bridge (DAB) converter to minimize the energy buffer in single-phase AC-DC converter applications. Single-phase converters commonly require bulky electrolytic capacitors due to their power pulsation at twice the grid frequency. However, the electrolytic capacitor often decreases the power density and lifetime of the power converter. Active power decoupling is one of the solutions to this problem by using a firm or ceramic capacitor as the energy buffer. However, the additional circuit decreases the conversion efficiency and power density.**

This paper proposes the active power decoupling method using a DAB converter without additional components. The Proposed method applies the feed-forward control to determine the phase shift angle for the power decoupling capability. In addition, the ZVS condition with the proposed method is considered to clarify the design of the small DC-link capacitor. The validity of the proposed method is demonstrated by the experimental result. As the experimental result, it was confirmed that the second harmonic component of the output voltage was reduced by 91.2%.

Keywords—Dual Active Bridge converter, Active power decoupling, carrier phase shift

I. INTRODUCTION

Electric Vehicles have been widely developed to reduce the carbon emissions of traditional gasoline vehicles. An onboard charger (OBC) is necessary to realize the battery charge from the AC grid, and it requires high conversion efficiency, small volume, and lightweight to implement on EVs.

OBC typically consists of an isolated AC-DC converter with a PWM rectifier and an isolated DC-DC converter. Candidates for isolated DC-DC converters include LLC converters, full bridge converters, and Dual Active Bridge (DAB) converters. DAB converters have been extensively studied due to their bi-directional power transfer and high-efficiency operation with Zero Voltage Switching (ZVS) owing to low switching losses.

OBC connects to a single-phase or three-phase AC grid. In single-phase applications, the single-phase power pulsation with twice the grid frequency should be eliminated from the output DC port because it may become a cause of the lifetime limitation of batteries [1]-[5]. Generally, a bulky electrolytic capacitor connects to the DC-link for the energy buffer of the single-phase power pulsation. However, electrolytic capacitors limit the reliability of the power converter. Moreover, this capacitor decreases the power density due to making a large capacitor bank by the low allowable ripple current.

An active power decoupling (APD) method is one of the solutions to replace the electrolytic capacitor in the single-phase converter [6]-[9]. This method eliminates the single-phase power pulsation from the DC port by a small capacitor such as a firm or ceramic capacitor. The simple APD implementation adds a boost or buck-type decoupling port to the DC link [10], [11]. However, the additional circuit may increase converter losses and circuit volume due to an increase of circuit components. The method of decoupling power without adding an active switch instead requires an additional capacitor across the bridge arm [12]. Therefore, a method that completely eliminates the need for additional components is required.

This paper proposes a power decoupling method by applying carrier phase shift control without extra components. This proposed method actively varied the phase shift angle according to the DC link voltage variation to obtain the constant DC power. This contribution of paper is that improvement of the power density owing to removing the bulky electrolytic capacitor without an extra APD circuit.

The remainder of the paper is organized as follows. Section II explains the circuit topology of the single-phase AC to DC and the principle of single-phase power pulsation. In section III, the proposed power pulsation compensation method is described. In addition, The ZVS range of DAB converters is presented. Finally, in section IV, the experimental results are demonstrated.

II. CIRCUIT TOPOLOGY AND PRINCIPLE OF SINGLE-PHASE POWER PULSATION

Fig. 1 shows a diagram of the isolated AC-DC converter under consideration. The isolated AC-DC converter consists of a circuit combining a PWM rectifier and a DAB converter. The

PWM rectifier has the DC-link voltage control and PFC capability for grid current. In contrast, the DAB converter has the transmission power control by the phase shift carrier control.

This circuit applies the small capacitors for C_{dc} and C_{out} to eliminate electrolytic capacitors. However, the second-order harmonics appear at DC-link voltage due to the small capacitance of C_{dc}. As a result, the transmission power fluctuates at the double-line frequency.

Fig. 2 shows the compensation principle of single-phase power pulsation. As shown in Fig. 2, the input power of a single-phase AC-DC converter pulsates at twice the frequency. In contrast, the output power is controlled constantly by charging and discharging the energy in the buffer capacitor C_{dc} to counteract input power pulsations. When both the Input voltage and current waveforms are sinusoidal, the relationship between instantaneous input power p_{in}, instantaneous output power p_{out}, and instantaneous power of the buffer p_{buf} is expressed as

$$p_{out} = p_{in} + p_{buf} = \frac{1}{2}V_{in}I_{in} - \frac{1}{2}V_{in}I_{in}\cos(2\omega t) + p_{buf} \quad (1),$$

where V_{in} is the peak voltage, I_{in} is the peak current and ω is the angular frequency of the input voltage. The second term in (1) shows the power pulsation component, which pulsates twice the input frequency. This power pulsation is superimposed on the DC link current as a ripple. When the instantaneous power is kept constant, the buffer instantaneous power p_{buf} to compensate for the input power pulsation is expressed as

$$p_{buf} = \frac{1}{2}V_{in}I_{in}\cos(2\omega t) \quad (2),$$

where the polarity of p_{buf} is positive when C_{buf} is charged. The first term in (1) is the DC amount, and the second term is the power pulsation component. The instantaneous power p_{buf} of the buffer is controlled to cancel the second term and is expressed as

$$p_{out} = \frac{1}{2}V_{in}I_{in} \quad (3).$$

The second and third terms in (1) cancel so that the output power is only the DC value shown in (3). Since the output power is constant, the output voltage is also constant when a load resistor is connected.

III. Proposed Power Decoupling Method.

A. Proposed control method

The proposed method controls the transmission power of the DAB converter to compensate for the twice-frequency power pulsations that occur in the DC link. First, the relationship between the phase difference and the transmission power of a typical DAB converter is explained. The relationship between the phase difference and output power P_{out} when the transformer voltage is set to two levels is expressed as

$$P_{out} = \frac{NV_{dc}V_{out}}{\omega L_2}\delta\left(1-\frac{\delta}{\pi}\right) \quad (4),$$

where V_{dc} and V_{out} are the DC link and output voltages, respectively, N is the turn ratio of the high-frequency transformer, and L_2 is the inductance value. It is the phase

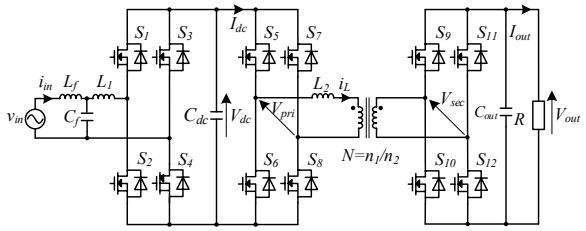


Fig. 1 Circuit configuration of isolated AC-DC converter using DAB converter.

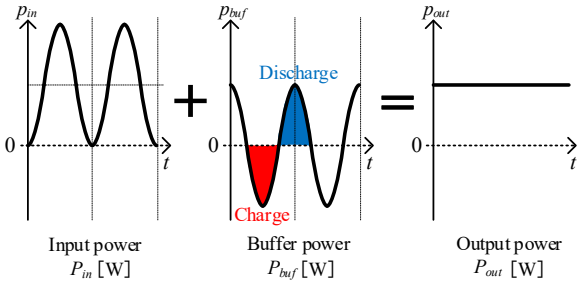


Fig. 2 Compensation principle of power ripple

difference between the primary and secondary of the DAB converter.

In the proposed circuit, the input voltage of the DAB converter pulsates at twice the frequency of the single-phase system. The DC link voltage $V_{dc,}$ including the pulsation, is expressed as

$$V_{dc} = V_{avg} + \Delta V_c \sin(2\omega t) \quad (5),$$

V_{avg} is the average voltage of the DC link voltage, and ΔV_c is the DC link voltage pulsation amplitude. From (4) and (5), the output power P_{out}, including single-phase pulsation, is expressed as

$$P_{out} = \frac{NV_{out}\{V_{avg} + \Delta V_c \sin(2\omega t)\}}{\omega L_2}\delta\left(1-\frac{\delta}{\pi}\right) \quad (6).$$

When the phase difference d is constant, the output power of the DAB converter pulsates at twice the frequency due to input voltage fluctuations in (6). Therefore, the proposed control actively varies the phase difference d to keep the output power constant. The phase difference of the DAB converter is expressed as

$$\delta = \frac{\pi}{2}\left(1-\sqrt{1-\frac{8P_{out}f_{sw}L_2}{NV_{dc}V_{out}}}\right) \quad (7),$$

where, the DC link voltage uses the instantaneous value to calculate the phase difference d of the DAB converter to compensate for single-phase power pulsations. Therefore, output power is controlled on an instantaneous power basis, which allows constant control of output power. The phase difference d to compensate for single-phase power pulsation is expressed as

$$\delta = \frac{\pi}{2}\left\{1-\sqrt{1-\frac{8P_{out}f_{sw}L_2}{NV_{out}\{V_{avg} + \Delta V_c \sin(2\omega t)\}}}\right\} \quad (8).$$

B. *Relationship between buffer capacitance and ripple voltage*

The amount of power to be compensated and the allowable fluctuation voltage of the capacitor determine the capacitor capacity for compensating single-phase power pulsation. The amount of power required to compensate for power pulsation *Wc* is expressed as

$$W_c = \frac{1}{2} V_{in} I_{in} \int_0^{\frac{1}{4f}} \sin(2\omega t)\, dt = \frac{V_{in} I_{in}}{2\omega} = \frac{p_{out}}{\omega} \tag{9}.$$

From the relationship between capacitor power and voltage, the amount of capacitor power is expressed as

$$W_c = \frac{1}{2} C V_{cmax}{}^2 - \frac{1}{2} C V_{cmin}{}^2 \tag{10},$$

where V_{cmax} is the maximum fluctuating voltage, and V_{cmin} is the minimum fluctuating voltage. From (9) and (10), the capacitance C_{buf} of the buffer capacitor used for single-phase power pulsation compensation is expressed as

$$C_{buf} = \frac{2P_{out}}{\omega\left(V_{cmax}{}^2 - V_{cmin}{}^2\right)} = \frac{P_{out}}{2\omega V_{avg} \Delta V_c} \tag{11}.$$

The output power and the capacitance of the buffer capacitor determine V_{cmax} and V_{cmin}. The addition of the average voltage V_{avg} and the fluctuating voltage ΔV_c of the voltage pulsation is V_{cmax}, and the subtraction is V_{cmin}. From (11), the fluctuating voltage ΔVc variation width and the buffer capacitor capacitance are inversely proportional.

C. *ZVS range of DAB converter*

This chapter investigates the ZVS range when the proposed single-phase power pulsation compensation is applied in a two-level DAB converter. To achieve ZVS over the entire operating range, even when the input voltage of the DAB converter pulsates due to single-phase power pulsation, the phase difference variation during APD operation should operate within the ZVS condition. Therefore, the ZVS range and circulating current in the proposed method are explained.

Fig. 3 shows the waveforms of the primary voltage v_{pri}, secondary voltage v_{sec}, and inductor i_L of the DAB converter. The condition for soft switching to be established in the DAB converter depends on the positive and negative inductor current i_L. Fig. 3 (a) shows the inductor current waveform when $i_L > 0$ in the interval from t_2 - t_3. Fig. 3 (b) shows that $i_L < 0$ at time t_2, and soft switching is not established when the mode switches. In Fig. 3(c), $i_L < 0$ at time t_3, and, as in Fig. 3(b), soft switching does not take place. Therefore, soft switching is established when both conditions $i_L > 0$ in the interval t_2 - t_3 and ZVS can be achieved.

The ZVS conditions for the inductor currents $i\ (t_2)$ and $i\ (t_3)$ are expressed as

$$i(t_2) = \frac{(2\delta - \pi)V_{dc} + \pi N V_{out}}{2\omega L} > 0 \tag{12},$$

$$i(t_3) = \frac{\pi V_{dc} + (2\delta - \pi) N V_{out}}{2\omega L} > 0 \tag{13},$$

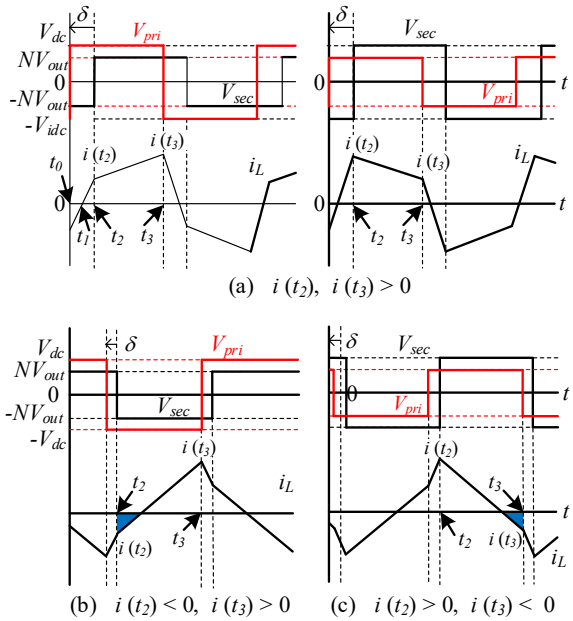


Fig. 3 Inductor current and soft switching success or failure

where the condition for a phase difference that can achieve ZVS is expressed as

$$\delta > \frac{\pi}{2}\left(1 - \frac{NV_{out}}{V_{dc}}\right) \tag{14},$$

$$\delta > \frac{\pi}{2}\left(1 - \frac{V_{dc}}{NV_{out}}\right) \tag{15}.$$

Therefore, the ZVS condition of the DAB converter when the input voltage pulsates is expressed as

$$\delta > \frac{\pi}{2}\left\{1 - \frac{NV_{out}}{V_{avg} + \Delta V_c \sin(2\omega t - \pi)}\right\} \tag{16},$$

$$\delta > \frac{\pi}{2}\left\{1 - \frac{V_{avg} + \Delta V_c \sin(2\omega t - \pi)}{NV_{out}}\right\} \tag{17}.$$

This section describes the phase difference due to the input voltage pulsation of the DAB converter during APD. From equation (8), the expressions for the phase difference when the DC link voltage is at its maximum and minimum values are expressed as

At maximum DC link voltage

$$\delta = \frac{\pi}{2}\left\{1 - \sqrt{1 - \frac{8 I_{out} f_{sw} L_2}{N(V_{avg} + \Delta V_c)}}\right\} \tag{18},$$

At minimum DC link voltage

$$\delta = \frac{\pi}{2}\left\{1 - \sqrt{1 - \frac{8 I_{out} f_{sw} L_2}{N(V_{avg} - \Delta V_c)}}\right\} \tag{19}.$$

The phase difference in (18) and (19) must follow the ZVS condition in (16) and (17).

Fig. 4 shows the ZVS range of the DAB converter and the operating point of the phase difference during APD. In this case, the average voltage V_{avg} of the DC link voltage is 1p.u. From (11), the DC link voltage fluctuation voltage increases when the buffer capacitor is made small. With a buffer capacitor of 150μF, ZVS operates in the entire range. However, with a buffer capacitor of 100μF, the fluctuating voltage of the DC link voltage increases, resulting in sections of hard switching. Therefore, a trade-off exists between smaller buffer capacitor capacitance and ZVS operation over the entire region. The maximum and minimum DC link voltages must be within the ZVS range to achieve both APD and ZVS operations over the entire range. The boundary conditions of the ZVS range are expressed as

ZVS boundary conditions at maximum input voltage

$$\sqrt{1-\frac{8I_{out}f_{sw}L_2}{N\left(V_{avg}+\Delta V_c\right)}} < \frac{NV_{out}}{V_{avg}+\Delta V_c} \quad (20),$$

ZVS boundary conditions at minimum input voltage

$$\sqrt{1-\frac{8I_{out}f_{sw}L_2}{N\left(V_{avg}-\Delta V_c\right)}} < \frac{V_{avg}-\Delta V_c}{NV_{out}} \quad (21).$$

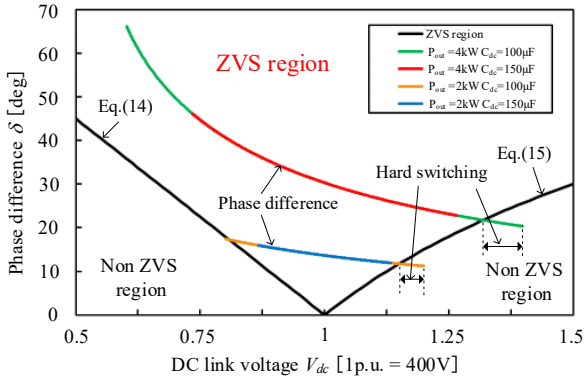


Fig. 4 Relationship between the ZVS range of DAB converter and the maximum and minimum DC link voltage pulsations.

IV. Experimental Results

In this chapter, the effectiveness of the proposed method is verified using a prototype with a rating of 4 kW under the experimental conditions shown in Table 1. The input voltage V_{in} is 200 V_{rms}, the output voltage V_{out} is 400 V, and the grid frequency f_g is 50 Hz.

Fig. 5 shows the relationship between the maximum possible ZVS variation voltage ΔV_c and buffer capacitor capacitance C_{buf} when output power P_{out} is varied. The range in which ZVS is possible at all operating points must satisfy ZVS boundary conditions in (20) and (21). As a result, the maximum fluctuating voltage for the DAB converter to operate ZVS in the full range at 4 kW output power is 125 V. From (11), the buffer capacitance is calculated to be 125 μF for a maximum fluctuating voltage of 125 V. In this experiment, the buffer capacitor C_{buf} was designed to be 150μF to keep the DC link voltage fluctuation voltage below 125V for ZVS operation in all regions.

Table.1 Experimental parameters

Parameter		
Rated Power	P_{out}	4kW
Grid voltage	v_{in}	200V_{rms}
Grid Frequency	f_g	50Hz
DC Link voltage	V_{dc}	400V
Output voltage	V_{out}	400V
Switching Frequency	f_{sw}	50kHz
Turn Ratio	N	n_1/n_2=1
Inductor (LC rectifer)	L_f	800μH
Inductor (PWM rectifer)	L_1	800μH
Inductor (DAB converter)	L_2	56μH
Capasitor (LC rectifer)	C_f	3nF
Buffer Capasitor	C_{dc}	150μF
Output Capasitor	C_{out}	60μF
Output Resistance	R	40 Ω
Cutoff Freq. of Current Control	f_{c_acr}	1kHz
Cutoff Freq. of Voltage Control	f_{c_avr}	10Hz

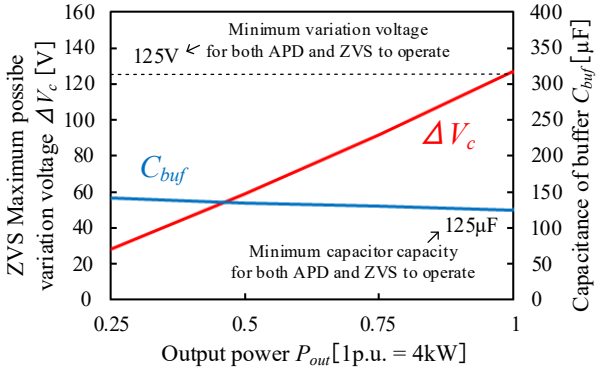
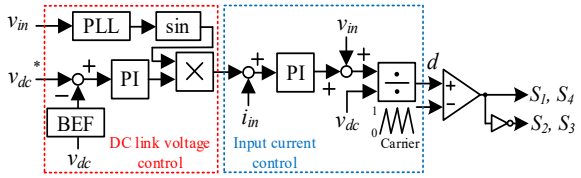
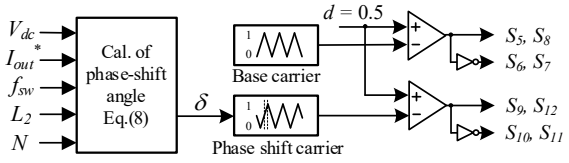


Fig.5 Maximum fluctuating voltage and buffer capacitor capacitance that can be ZVS over the entire range due to output power change.

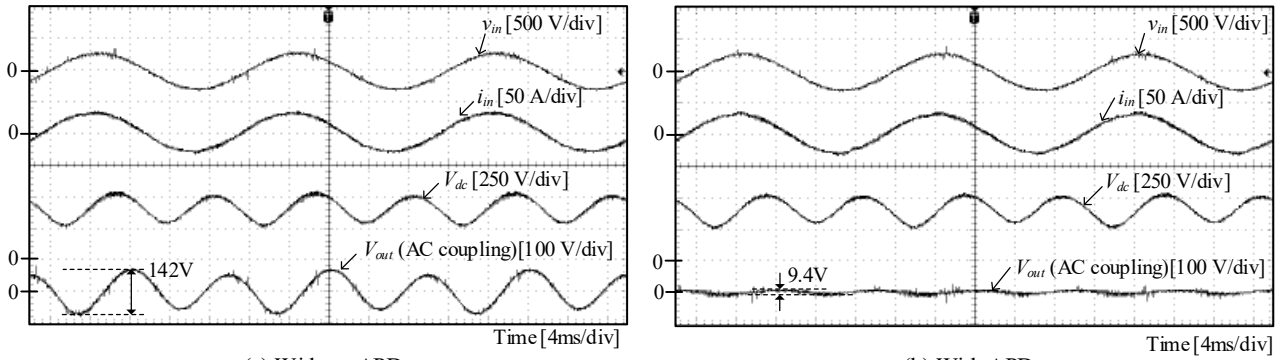


(a) Control block diagram of PWM rectifier



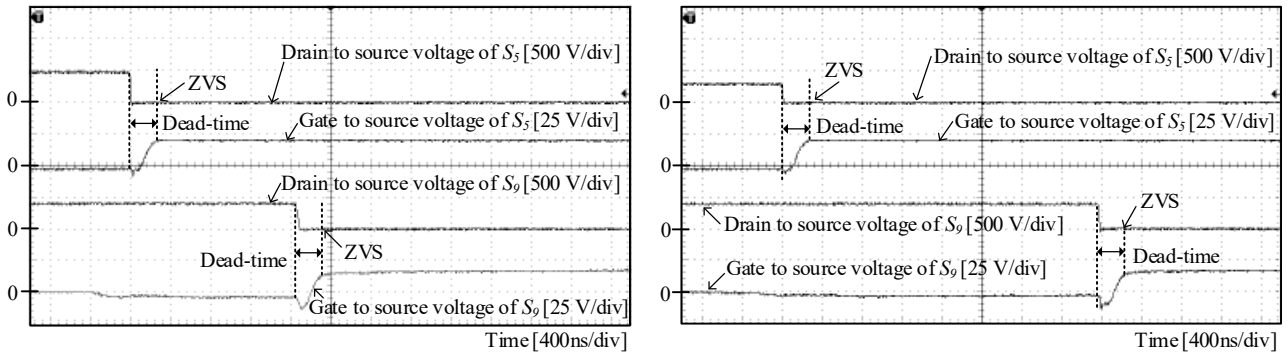
(b) Control block diagram of DAB converter

Fig. 6 Control block diagram for the isolated AC-DC converter.



(a) Without APD (b) With APD

Fig.7 Experiment result of proposed power decoupling control.



(a) Maximum DC link voltage (b) Minimum DC link voltage

Fig.8 Gate to source voltage and drain to source voltage of S_5 and S_9 at the DAB converter

Fig.6 shows the control block diagram of the proposed circuit. Fig. 6 (a) and Fig. 6 (b) show the control block diagrams of the PWM rectifier and DAB converter. The PWM rectifier controls the average value of the DC link voltage. The DAB converter performs carrier phase shift control using the phase difference calculated from (8). where using the detected value in the DC link voltage term of (8) allows feed-forward control even when the load conditions change.

Fig.7 shows the experimental waveforms to confirm the validity of the proposed APD method. The output voltage was measured with AC decoupling to verify the effect of reducing the second harmonic component. According to Fig.7 (a), the DC voltage fluctuation of 142V occurs due to the power ripple. On the other hand, The proposed APD method eliminates the low-frequency harmonics on the DC voltage and reduces the load voltage fluctuation by 93.4%, as shown in Fig. 7 (b). Moreover, the sinusoidal input current is obtained by the PFC control.

Fig.8 shows the drain-source voltage and gate-source voltage of the DAB converter. Fig.8 (a) and Fig.8 (b) show the switching waveforms at the maximum and minimum DC link voltages, respectively. The phase difference was operated based on the ZVS range to achieve both APD and ZVS. in Fig.4.

Fig.9 shows the harmonic analysis result of the DC output voltage. The ratio of each harmonic to the DC component with and without the proposed APD method is shown. According to Fig.9, Compensation for power pulsation reduced the second harmonic component by 91.2%. Therefore, power decoupling

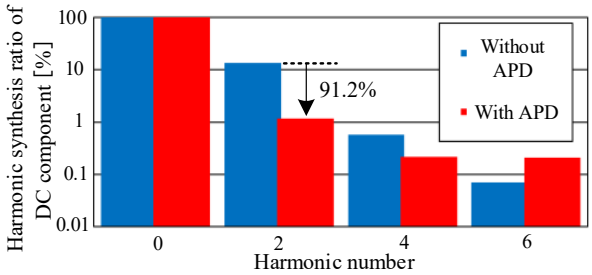


Fig.9 Harmonic analysis result of output voltage

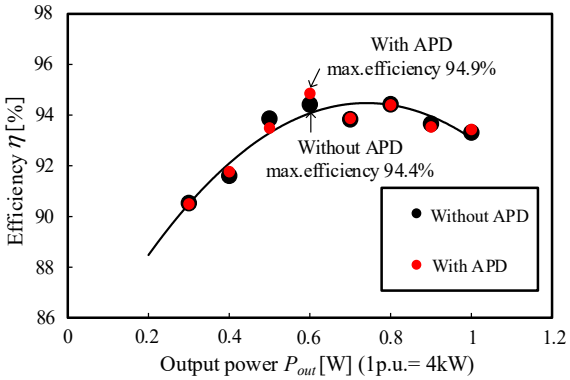


Fig. 10 Efficiency characteristic

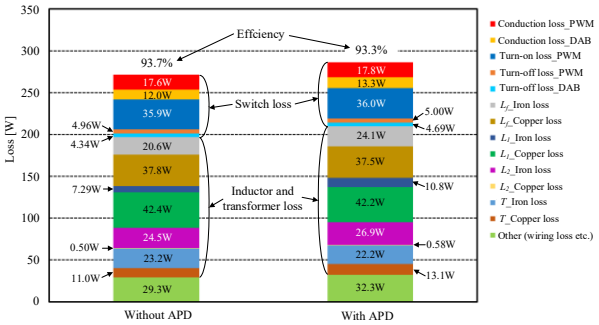


Fig.11 Loss analysis result with and without APD control.

was achieved by controlling the phase difference of the DAB converter.

Fig.10 shows the efficiency curves of the isolated AC-DC converter. According to Fig.10, the efficiency with the proposed APD is the same as the efficiency without APD. This is because the DAB converter operates in ZVS even during APD operation, which reduces switching losses.

The efficiency of this prototype is low at 93.3%. This could be due to pulsating DC link voltage. The DAB converter is based on the condition that the input-to-output voltage ratio and the transformer turn ratio match, and the effective value of the transformer current increases as the voltage varies. Therefore, under the parameter conditions of this paper, the large fluctuations in DC link voltage with and without APD increase the RMS value of transformer current and reduce efficiency.

Fig. 11 shows the results of loss separation with and without the proposed APD. The overall loss is divided into switch loss, inductor loss, and transformer loss, respectively. The losses that occur in a switch are divided into conduction losses and switching losses. The conduction loss was derived by the product of the square of the current RMS value and the winding resistance. The switching losses were derived from the turn-on and turn-off losses from the data sheets of the MOS-FET (SCT4018KR : Rohm), used in the experiments. At that time, the turn-on loss is assumed to be zero because the DAB converter operates ZVS on all switches. Separate inductor and transformer losses into iron and copper losses. The copper loss was derived by the product of the square of the current RMS value and the inductor or transformer wiring resistance. The iron loss was derived by subtracting the copper loss from the total loss of each inductor and transformer. Wiring losses and reactive power losses are considered as other losses.

The conduction, switching, iron, and copper loss with APD increased more than without APD in Fig.11. However, the increase in loss due to APD adaptation is only 0.28% of the total power and does not significantly affect the overall circuit loss. The iron and copper losses in the inductors and transformers account for about 61.9% of the total loss. In addition, the inductor on the input side of the PWM rectifier has a large ratio of iron loss to copper loss. Therefore, the optimal design of the inductor of the PWM rectifier may improve the overall efficiency of the circuit.

V. Conclusion

This paper proposed the APD method for DAB converters based on carrier phase shift control, and it does not require additional circuits. The proposed method compensates for the power pulsation by controlling the phase difference of the DAB converter to cancel the double-frequency pulsation occurring in the single-phase system. This method maintains constant output power with a small-capacity DC link capacitor. The conditions for ZVS corresponding to power pulsation compensation were also studied, and boundary conditions that allow ZVS in all regions were derived. The conditions for ZVS that are compatible with power pulsation compensation were also investigated. The experimental result showed that the pulsation of the output voltage was reduced by 93.4%. The operation of the proposed APD method was compatible with the ZVS operation of the DAB converter in its entire operating range. The efficiency improvement will be considered based on loss analysis in future work.

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