Three/Single-Phase Switchable DAB Matrix Converter and Active Power Decoupling Method with Center-Tapped Transformer

Kousei Irimura
Department of Science of Technology Innovation
Nagaoka University of Technology
Nagaoka, Japan
s223133@stn.nagaokaut.ac.jp

Masamichi Yamaguchi
Department of Science of Technology Innovation
Nagaoka University of Technology
Nagaoka, Japan
m_yamaguchi@stn.nagaokaut.ac.jp

Hiroki Watanabe
Department of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Japan
hwatanabe@vos.nagaokaut.ac.jp

Jun-ichi Itoh
Department of Science of Technology Innovation
Nagaoka University of Technology
Nagaoka, Japan
itoh@vos.nagaokaut.ac.jp

***Abstract*— This paper proposes a Dual Active Bridge (DAB)-type matrix converter capable of supporting both three-phase and single-phase grid connections. In single-phase systems, power ripple is actively compensated by controlling a buffer circuit connected to the transformer center tap during the inverter's zero-voltage period, eliminating the need for additional switching devices. A control method based on common-mode pattern switching is introduced to regulate the buffer current. Simulation results demonstrate high power factor:0.99 and 97% reduction in the power ripple component of the DC current without using lookup tables. The proposed approach also reduces component count, making it suitable for compact and reliable onboard charger applications.**

Keywords*— *Dual Active Bridge (DAB), Matrix converter, Power ripple compensation, Single-phase grid, Onboard Charger (OBC)

I. INTRODUCTION

In recent years, the demand for electric vehicles (EVs) has rapidly increased due to growing concerns of global warming. In addition, the utilization of the power storage capability of EVs has been proposed for grid systems [1][2]. A compact and bidirectional onboard charger (OBC) is required for the effective integration of EV batteries into the grid. Then, an isolated AC-DC converter, which interfaces with both three-phase and single-phase systems, is desirable.

In particular, compensation for power ripple generated at twice the line frequency is necessary in a single-phase grid-tied converter. Although a passive ripple compensation using a large smoothing capacitor is commonly employed for power ripple compensation, passive method requires electrolytic capacitor with short lifespans, which reduces the reliability of the OBC.

On the other hand, Active Power Decoupling (APD) is a method for power ripple compensation that enables the use of a small buffer capacitor. APD actively controls the current of the buffer capacitor by using semiconductor switches. Because APD does not require a large buffer capacitor, electrolytic capacitor with short-lifespan is not necessary. Various APD topologies, which are applicable to both three-phase and single-phase systems, have been proposed [4][5].

Reference [4] proposes an OBC that employs an interleaved totem-pole type isolated AC-DC converter consisting of three parallel-connected modules. In three-phase systems, sinusoidal outputs with 120-degree phase shifts are generated to balance the load across the three phase, thereby supporting high-capacity charging. In single-phase systems, two modules are used for power conversion, while the remaining module operates as a buffer circuit to compensate for ripple components. The approach achieves Zero Voltage Switching (ZVS) is achieved for all switches, and active power decoupling (APD) is realized by simply adding a buffer capacitor. However, the use of two buffer inductors connected in series with the transformer and the buffer capacitor is required for ripple compensation. The additional components increase circuit complexity and volume.

Reference [5] proposes a resonant AC–DC converter that employs a three-phase to single-phase matrix converter. During single-phase operation, active power decoupling (APD) is realized by using the unused phase switches and the grid-side filter capacitors for ripple compensation, without increasing the number of components. However, a nonlinear relationship exists between the current reference and the switching operation. The current reference corresponds to either the grid current or the transformer current. Thus, the nonlinear relationship requires the use of a lookup table. In addition, using the filter capacitors for APD causes a significant drop in power factor under light-load conditions.

Therefore, this paper proposes a three-phase to single-phase matrix converter based on a Dual Active Bridge (DAB) topology. The proposed converter performs power ripple compensation during single-phase operation. A center-tapped transformer is employed in the circuit configuration. By connecting a buffer circuit to the center tap, active power decoupling is realized without the need for additional switching devices. Because the buffer circuit operates independently from the power system, the converter enables bidirectional power transfer while maintaining a high power factor. The effectiveness of ripple suppression during single-phase operation is demonstrated in both motoring and regenerating modes through simulation analysis.

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II. Proposed Circuit

A. Circuit configuration

Fig. 1 shows the configuration of the proposed converter, which is based on a DAB topology for three-phase to single-phase conversion. The proposed converter employs a center-tapped transformer. The primary winding of the transformer is connected to the power grid through a matrix converter. Direct AC–AC conversion by the matrix converter eliminates the need for a boost inductor, a DC-link capacitor, and a pre-charging circuit. The secondary winding of the transformer is connected to an inverter. A buffer circuit, consisting of an inductor and a capacitor, is connected to the center tap of the transformer. Because the buffer circuit does not include additional switching devices, the total number of components in the system is reduced.

B. Control method with three-phase grid

In the matrix converter used in the proposed circuit, grid current control is applied through Space Vector Modulation (SVM) [6] based on a three-phase system. Because the proposed converter employs a DAB configuration, the instantaneous current flowing through the transformer does not remain constant. Therefore, the duty ratios calculated from SVM cannot be directly used. Modified duty ratios must be derived to generate the current vectors I_1 and I_2 that are specified by SVM.

Fig. 2 shows the output voltages of the matrix converter and the inverter under a three-phase system, along with the transformer current waveform. The output durations within one switching period and their corresponding ratios are defined as T_a, T_1, T_2, T_b, and T_0, and D_a, D_1, D_2, D_b, and D_0, respectively. The instantaneous transformer current values at each duration are defined as i_1, i_2, and i_3. Under the assumption that the initial current i_0 is zero, the relationship between each current value and the current vectors obtained by SVM is expressed by

$$\begin{cases} I_1 = \dfrac{i_1}{2} D_a + \dfrac{i_1 + i_2}{2} D_1 \\ I_2 = \dfrac{i_2 + i_3}{2} D_2 \end{cases} \quad \text{.....(1).}$$

Each duty ratio is derived by substituting the leakage inductance and each output voltages into (1). Each duty ratio is derived as

$$D_1 = \sqrt{\frac{4 I_1 L f_{sw}}{v_{\max}(a+1)^2 - N V_{dc}}}, \quad D_2 = \left(-b \pm \sqrt{b^2 - 4c}\right)\frac{D_1}{2}$$
$$D_b = \frac{\left(v_{\max}(a+1) - N V_{dc}\right) D_1 + \left(v_{mid} - N V_{dc}\right) D_2}{N V_{dc}} \quad \text{.....(2),}$$
$$\because a = \frac{D_a}{D_1}, \; b = \frac{v_{\max}(a+1) - N V_{dc}}{v_{mid} - N V_{dc}}, \; c = \frac{I_2}{I_1}\frac{v_{\max}(a+1)^2 - N V_{dc}}{v_{mid} - N V_{dc}}$$

where $v_{\max}$ is the maximum line-to-line voltage, and v_{mid} denotes the intermediate line-to-line voltage. The coefficient a is a parameter determined by the output power and the DC voltage.

III. Proposed Operation With Single-Phase Grid

A. DAB operation for power transmittion

Under single-phase grid connection, the matrix converter is controlled based on virtual AC–DC–AC conversion [8]. A virtual PWM rectifier performs the rectification process

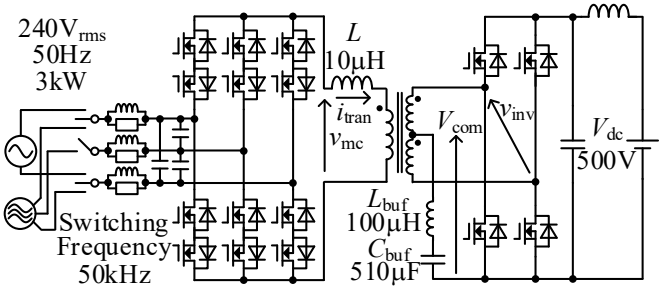

Fig. 1. Proposed isolated DAB-type AC-DC converter.

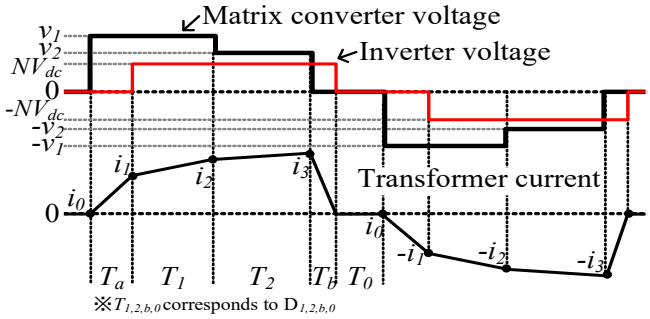

Fig. 2. High-frequency voltage and current waveforms.

synchronized with the grid voltage. Power transfer in a DAB configuration is achieved by combining a virtual inverter operating in two-level mode and a secondary-side inverter operating in three-level mode. The virtual inverter in the matrix converter generates a two-level rectangular waveform whose amplitude matches the grid voltage amplitude.

B. Zero voltage period on secondary side inverter

Around the zero-crossing point of the grid voltage, the amplitude difference between the primary and secondary voltages of the transformer becomes large. The increased amplitude difference causes a high-peak in the transformer current. Thus, the zero-voltage period of the secondary-side inverter is determined by the grid and the DC-side voltage. The duration of the zero-voltage period is calculated by

$$\varepsilon = T_{sw}\left|\frac{N V_{dc} - \sqrt{2} V_g \sin(\omega_0 t)}{\sqrt{2} V_g}\right| \quad \text{.....(3),}$$

where e denotes the zero-voltage period, N is the turns ratio of the transformer, T_{sw} is the switching period, and V_{g} is the root mean square value of the grid voltage. The calculated zero-voltage period suppresses the peak value of the transformer current and the reactive current around the zero-crossing point of the grid voltage.

C. Buffer current command for power ripple compensation

Under single-phase grid connection, power ripple compensation is necessary. The proposed converter performs ripple compensation using the buffer circuit connected to the center tap on the secondary side of the transformer. Fig. 3 illustrates the relationship among input power, output power, and buffer power during power ripple compensation. Assuming unity power factor in the single-phase system, the instantaneous input power is expressed by

$$\begin{aligned} p_{grid} &= 2 V_g I_g \sin^2(\omega_0 t) \\ &= V_g I_g - V_g I_g \cos(2\omega_0 t) = P_{ave}\{1 - \cos(2\omega_0 t)\} \end{aligned} \quad \text{.....(4),}$$

where V_g and Ig represent the root mean square values of the grid voltage and current respectively, P_{ave} denotes the average output power, and ω is the angular frequency of the grid. The power ripple corresponds to the second term in (4). Thus, required power compensated amount by the buffer circuit is defined by

$$p_{buf} = P_{ave}\cos(2\omega_0 t) \quad \text{.....(5),}$$

The polarity of p_{buf} is defined as positive when the buffer capacitor C_{buf} is being charged.

The buffer current i_{buf} and the buffer capacitor voltage v_{cbuf}, which control a buffer power, are calculated based on the charging energy of the buffer capacitor. The stored energy W_{cbuf} in the buffer capacitor is expressed using (4) and the voltage–current relationship of the capacitor by

$$\begin{aligned} W_{cbuf} &= \int_{t_0}^{t} V_{cbuf} i_{buf} d\tau = \int_{t_0}^{t} V_{cbuf}\left(C_{buf}\frac{dV_{cbuf}}{d\tau}\right)d\tau \\ &= \int_{t_0}^{t} P_{ave}\cos(2\omega_0 t)d\tau \end{aligned} \quad \text{.....(6),}$$

where t_0 denotes the initial operation time. Assuming that t_0 is zero and the initial voltage of the buffer capacitor is V_{co}, the buffer capacitor voltage is derived as

$$V_{cbuf} = \sqrt{V_{c0}^2 + \frac{P_{ave}}{\omega_0 C_{buf}}\sin(2\omega_0 t)} \quad \text{.....(7).}$$

The reference value for the buffer current is calculated from (7) and the voltage–current relationship of the capacitor as

$$i_{buf}^{*} = \frac{P_{ave}^{*}\cos(2\omega_0 t)}{\sqrt{V_{c0}^2 + \frac{P_{ave}^{*}}{\omega_0 C_{buf}}\sin(2\omega_0 t)}} \quad \text{.....(8),}$$

where P_{ave}^{*} is the reference value of the output power. The proposed circuit achieves power ripple compensation by controlling the buffer current i_{buf} to follow its command i_{buf}^{*}.

D. Power ripple compensation with center tap transformer

The secondary-side inverter operates in three-level mode in the proposed converter. The three-level operation generates a zero-voltage period on the secondary side of the transformer, as derived in (3). The buffer circuit is controlled during the zero-voltage period to allow compensation of power ripple without interfering with the power transfer operation.

Fig. 4 illustrates the current paths in the proposed method for power ripple compensation. Fig. 4(a) and 4(b) show operating patterns in which voltage is applied to the secondary winding of the transformer. These operating conditions are defined as differential patterns that contribute to power transfer. The voltage at the transformer center tap is equal to the voltage at the DC-side neutral point. Therefore, the buffer circuit remains unaffected during differential patterns.

Fig. 4(c) and 4(d) show operating patterns in which the voltage applied to the transformer secondary is zero. These patterns are defined as common-mode patterns that do not contribute to power transfer. Although the transformer current does not change due to the zero voltage on the secondary winding, either a DC voltage or zero voltage appears at the center tap. Thus, the center tap voltage is controlled by switching between the two common-mode patterns. The buffer current control, which allows the power ripple

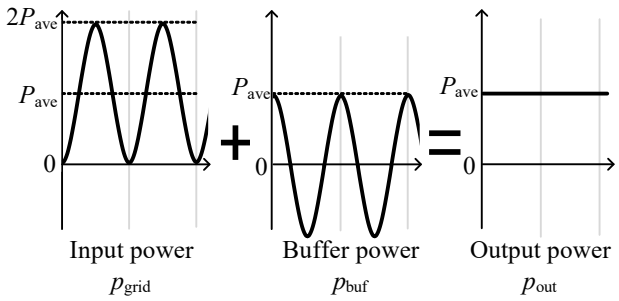

Fig. 3. Principle of Power Pulsation Compensation.

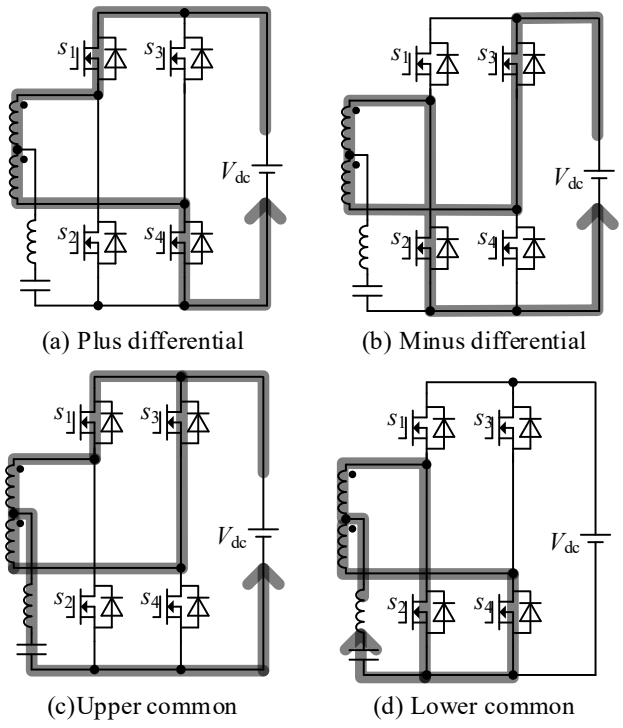

Fig. 4. Configuration of the pattern for the DC side.

compensation, is achieved by the control of the center tap voltage.

Fig. 5 shows the transformer voltage waveform of the matrix converter and the inverter, along with an outline of the center tap voltage during motoring operation. The common-mode operation is configured to alternate charging and discharging of the buffer capacitor within one control cycle of the secondary-side inverter. The average value of the center tap voltage is defined by

$$V_{com} = \left(\frac{V_{dc}}{2}T_1 + \frac{V_{dc}}{2}T_2 + V_{dc}T_{zp} + 0\cdot T_{zn}\right)\frac{1}{T_{sw}} \quad \text{.....(9),}$$

where T_{zp} represents the charging duration of the buffer capacitor in the common-mode operation, T_{zn} is the discharging duration, and T_{sw} denotes the switching period. The total duration of the common-mode operation, which is the sum of T_{zp} and T_{zn}, coincides with the zero-voltage period determined by (3). The differential-mode output durations T_1 and T_2 must be equal to ensure that the voltage–time integral of the transformer is equal to zero. Additionally, the total

duration of the differential-mode and common-mode patterns must match the switching period. The constraint conditions for these durations are defined by

$$\begin{aligned} T_{zp}+T_{zn}&=\varepsilon \\ T_1-T_2&=0 \\ T_1+T_2+T_{zp}+T_{zn}&=T_{sw} \end{aligned} \quad \text{.....(10).}$$

By substituting the (10) into (9), the output durations of each mode required to realize the commanded center tap voltage are derived as

$$T_1=T_2=\frac{T_{sw}-\varepsilon}{2} \quad \text{.....(11).}$$

$$T_{zp}=\frac{\varepsilon}{2}-\frac{T_{sw}}{2}+\frac{V_{com}^*}{V_{dc}}T_{sw}$$

$$T_{zn}=\frac{\varepsilon}{2}+\frac{T_{sw}}{2}-\frac{V_{com}^*}{V_{dc}}T_{sw}$$

E. Derivation of the phase shift equation

Fig. 6 shows the transformer voltage and current waveforms of the matrix converter and the secondary-side inverter during motoring operation. In the example shown, the output durations of the charging and discharging modes are equal, and the phase shift between the primary and secondary sides is smaller than half of the zero-voltage period. Because the grid frequency is significantly lower than the switching frequency of the matrix converter, the output voltage of the matrix converter can be considered constant within one control cycle of the secondary-side inverter.

The active power of the DAB is calculated as the control-cycle average of the product of the transformer current area under each operating condition and the output voltage of the secondary-side inverter. The instantaneous transformer current for each operating mode, referenced from the initial current i_0, is expressed by

$$\begin{cases} i_1=i_0+\dfrac{|v_{grid}|}{L}\delta \\ i_2=i_1+\dfrac{|v_{grid}|-NV_{dc}}{L}T_1 \\ i_3=i_2+\dfrac{|v_{grid}|}{L}\left(\dfrac{T_{sw}}{2}-\delta-T_1\right) \\ i_4=i_3+\dfrac{-|v_{grid}|}{L}\left(T_{zp}-\dfrac{T_{sw}}{2}+\delta+T_1\right) \\ i_5=i_4+\dfrac{-|v_{grid}|+NV_{dc}}{L}T_2 \\ i_6=i_5+\dfrac{-|v_{grid}|}{L}\left(T_{zn}-\delta\right) \end{cases} \quad \text{.....(12),}$$

where L denotes the sum of the leakage inductance and additional inductance of the transformer, and d represents the phase shift between the primary and secondary sides of the transformer. Based on (12), the average power is calculated, and the relationship among transmitted power, the zero-voltage period, and the phase shift is obtained as

$$p=\frac{NV_{dc}|v_{grid}|}{T_{sw}L}T_{diff}\left(2T_{diff}+T_{zp}+2\delta-T_{sw}\right) \quad \text{.....(13),}$$

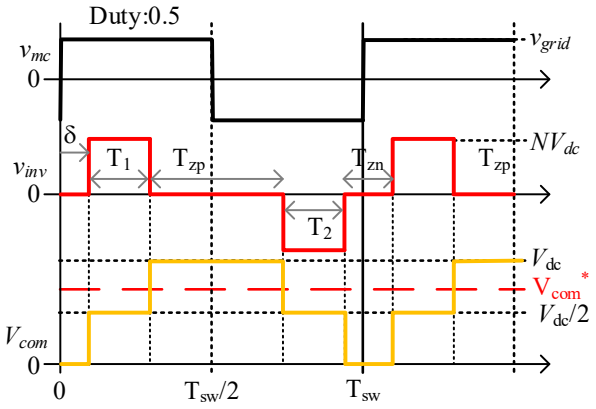

Fig. 5. Control block diagram. The zero-voltage period is calculated from the neutral-point voltage.

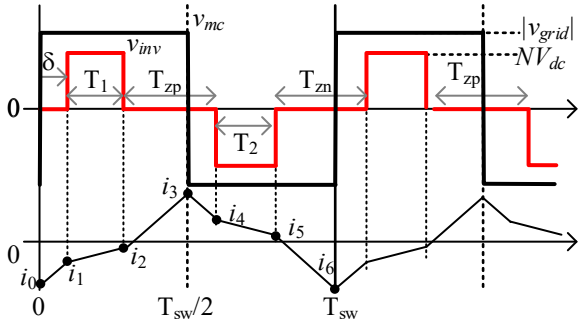

Fig. 6. Transformer voltage and current waveforms with a phase-difference.

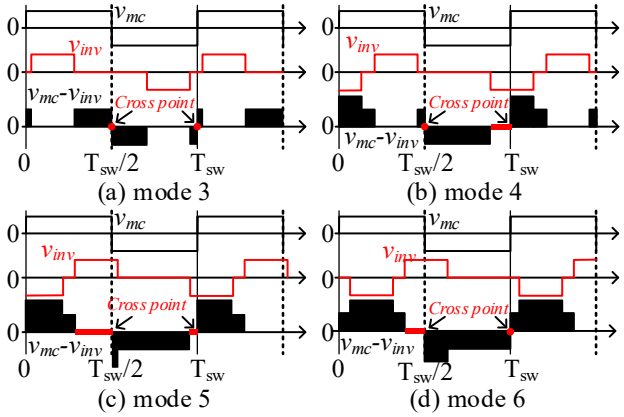

Fig. 7. The transformer voltage waveform varies depending on the conditions of phase difference and zero voltage period.

where T_{diff} represents the output time of the differential mode, which is equal to both T_1 and T_2. Furthermore, by solving for the phase shift using (13) and applying the result to (14), the phase shift is expressed by

$$\delta=\frac{1}{2}\left(T_{sw}-2T_{diff}-T_{zp}\right)+\frac{1}{2T_{diff}}\frac{T_{sw}L}{NV_{dc}\times|v_{grid}|}p \quad \text{..... (14)[8].}$$

By applying the derived phase shift δ, the desired transmitted power is maintained even when the zero-voltage period becomes unbalanced due to power ripple compensation.

F. Several phase shift equations considered the zero-voltage period imbalance

In the proposed control method, the output durations of the charging and discharging modes are not always balanced. As a result, various current modes occur beyond the operating condition shown in Fig. 6. By excluding boundary conditions

and assuming that the phase shift per control cycle is less than 180 degrees, a total of ten current modes are identified. Table 1 summarizes the determination conditions, and phase shift expressions for each current mode. These expressions are derived using the same procedure described in (13) and (14). The condition for selecting each phase shift equation depends on the phase shift itself. Therefore, recursive computation is required. To avoid this complexity, the phase shift value from the previous sampling is used to evaluate the selection conditions.

Modes 1 and 2 occur when the center tap voltage is precisely half of the DC voltage and the difference in output durations between charging and discharging does not exceed the inverter-side dead time. Specifically, Mode 1 applies if half of the zero-voltage interval exceeds the phase shift, whereas Mode 2 applies if the phase shift is longer than that interval.

Fig. 7 shows the transformer voltage waveforms on both the primary and secondary sides for current modes 3 to 6. Modes 3 through 6 arise when the center tap voltage exceeds half of the DC voltage, such that the charging duration is longer than the discharging duration. Assuming equal voltage amplitudes on the primary and secondary sides, the relative switching timings produce a differential (primary–secondary) waveform whose polarity, pulse width, and inversion timing vary among these modes. Mode 3 generates a symmetric waveform around the midpoint of the switching half-cycle, whereas Modes 4 through 6 exhibit increasing asymmetry and distinct inversion timings.

Modes 7 through 10 are the converse of Modes 3 through 6, emerging when the discharging duration exceeds the charging duration. These modes are similarly characterized by their phase-shift conditions and the polarity-inversion timing of the differential voltage.

IV. Simulation

Table 2 summarizes the simulation conditions for the proposed circuit. The simulation is based on a European single-phase grid and is configured to achieve 3 kW power transfer to an EV battery. The magnetizing inductance of the transformer is set significantly higher than the additional inductance, and the on-resistance of the switching devices is set to 10 mΩ.

Fig. 8 shows the simulation waveforms. The grid power factor is 0.99, and the total harmonic distortion (THD) of the grid current up to the 40th harmonic is 0.79%. The buffer current tracks the reference waveform, with a maximum current ripple of 21 A_{peak}.

Fig. 9 presents the frequency analysis of the DC current. The proposed circuit reduces the 100 Hz ripple component by 97%. This result demonstrates the effectiveness of the proposed power ripple compensation method.

V. Conclusion

This paper proposed a Dual Active Bridge (DAB)-type matrix converter that supports both three-phase and single-phase grid connections and actively compensates for power ripple in single-phase systems. The proposed method compensates for power ripple by controlling a buffer circuit connected to the transformer center tap during the zero-voltage period of the inverter. This control enables power ripple compensation without the need for additional switching devices. At the same time, power transfer is realized through the phase shift between the primary and secondary sides of the transformer. Simulation results demonstrate that the proposed method achieves a high power factor without relying on lookup tables and reduces the number of components compared to conventional circuits.

Future work includes experimental validation of the proposed method under single-phase grid connection. Further investigations will focus on suppressing surge currents during the zero-crossing of the grid voltage, replacing buffer inductors with transformer leakage inductance, and expanding

Table 1. List of phase difference equations for each current mode.

Mode	Discriminant	Phase-difference equations
	Tzp = Tzn	
1	$\delta_Z < T_z$	$\delta = \frac{1}{2}\left(T_{sw} - 2T_{diff} - T_{zp} + {}^{x}\!/_{T_{diff}}\right)$
2	$\delta_Z > T_z$	$\delta = \frac{1}{2}\left(T_{sw} - T_{diff}\right) + \frac{1}{2}\sqrt{D_1 - 2x}$
	Tzp > Tzn	
3	$\delta_Z < T_{zn}$	$\delta = \frac{1}{2}\left(T_{sw} - 2T_{diff} - T_{zp} + {}^{x}\!/_{T_{diff}}\right)$ Same as Mode1
4	$\delta_Z + T_{diff} < \frac{T_{sw}}{2}$	$\delta = \frac{1}{2}\left(T_{sw} + T_{zn} - T_{zp}\right) - \frac{1}{2}\sqrt{D_2 - 4x}$
5	$\delta_Z + T_{diff} > \frac{T_{sw}}{2}$	$\delta = \frac{1}{2}\left(T_{sw} + T_{diff} + \frac{T_{zn}}{2} - \frac{T_{zp}}{2}\right) - \frac{1}{4}\sqrt{D_3 - 8x}$
6	$\delta_Z - T_{zn} - T_{diff} > 0$	$\delta = \frac{1}{2}\left(T_{sw} - 2T_{diff}\right) - \sqrt{T_{diff}^2 + T_{zn}T_{diff} - x}$
	Tzp < Tzn	
7	$\delta_Z + T_{diff} + T_{zp} < \frac{T_{sw}}{2}$	$\delta = \frac{T_{sw}}{2} - 2T_{diff} - T_{zp} - \sqrt{T_{diff}^2 + T_{zn}T_{diff} - x}$
8	$\delta_Z + T_{diff} < \frac{T_{sw}}{2}$	$\delta = \frac{1}{2}\left(T_{sw} - 2T_{diff} - T_{zp}\right) + \frac{x}{2T_{diff}}$
9	$\delta_Z + T_{diff} > \frac{T_{sw}}{2}$	$\delta = \frac{T_{sw}}{2} - \sqrt{T_{diff}^2 + T_{zp}T_{diff} - x}$
10	$\delta_Z > T_{zn}$	$\delta = \frac{1}{2}\left(T_{sw} - T_{diff} + \frac{T_{zn}}{2} - \frac{T_{zp}}{2}\right) - \frac{1}{4}\sqrt{D_4 - 8x}$
Given	$x = power \times \mathrm{T_{sw}} L / \left(NV_{dc} \times \lvert v_{grid} \rvert\right)$ $D_1 = 2T_{sw}\left(T_{diff} + T_{zp}\right) - \frac{1}{2} - T_{diff}^2 - 2T_{diff}T_{zp} - 2T_{zp}^2$ $D_2 = T_{sw}\left(2T_{zn} + 2T_{zp} + 4T_{diff}\right) - \left(1 + \left(T_{zp} + T_{zn}\right)^2 + 4T_{diff}T_{zp}\right)$ $D_3 = T_{sw}\left(8T_{diff} + 4T_{zn} + 4T_{zp}\right) + K$ $K = -2T_{sw}^2 - 4T_{diff}\left(T_{diff} - T_{zn} - T_{zp}\right) - 3T_{zn}^2 - 2T_{zn}T_{zp} - 3T_{zp}^2$	

Table 2 Simulation parameter.

Simulation conditions	Symbol	Value
Switching frequency	f_{sw}	50 kHz
Transition power	P_{ave}	3 kW
Grid voltage	v_{ac}	240 V_{RMS}
Grid frequency	f_g	50 Hz
DC-source voltage	V_{dc}	500 V
Buffer capacitor	C_{buf}	510 μF
Buffer Inductor	L_{buf}	100 μH
Leakage inductor	L	10 μH
Trun ratio(Primary:Secondary)		0.6:(1:1)

the operating range of zero-voltage switching. These approaches aim to further reduce the circuit size and improve overall efficiency.

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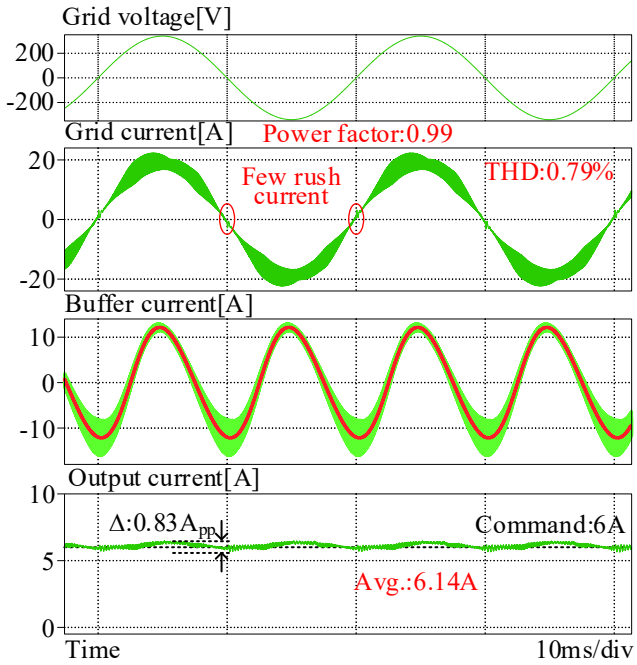

Fig. 8 Simulation results for 3kW.

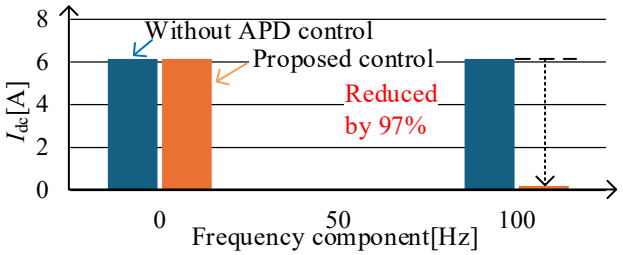

Fig. 9 Output current frequency analysis results.