Current Balancer Integrated with Impedance Matching Circuit for Megahertz High-power WPT Systems

Masamichi Yamaguchi
Department of Science of Technology Innovation
Nagaoka University of Technology
Nagaoka, Japan
m_yamaguchi@stn.nagaokaut.ac.jp

Hiroki Watanabe
Department of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Japan
hwatanabe@vos.nagaokaut.ac.jp

Jun-ichi Itoh
Department of Science of Technology Innovation
Nagaoka University of Technology
Nagaoka, Japan
itoh@vos.nagaokaut.ac.jp

***Abstract*— This paper proposes a novel current balancer integrated with an impedance-matching circuit for megahertz-range Wireless Power Transfer (WPT) systems. The proposed balancer achieves current sharing between parallel-connected inverters on the transmission side without requiring any additional control. The effect of the current balancing mechanism is analytically investigated, and the current imbalance rate is derived. Simulation results verify the accuracy of the derived expression for the current imbalance rate. Furthermore, the proposed balancer, combined with an additional capacitor, constitutes an impedance-matching circuit that enables Zero Voltage Switching (ZVS) in each parallel-connected inverter. Experimental results obtained from a prototype demonstrate successful ZVS operation. Finally, the inverter system with the proposed balancer achieves an input power of 6.5 kW at 6.78 MHz.**

Keywords*— current balancing, wireless power transfer, high-frequency power converter, transformer

I. Introduction

In recent years, battery chargers have been actively developed due to the growing interest in small mobility applications such as micro electric vehicles, autonomous delivery robots, and drones. Among the various charging methods, Wireless Power Transfer (WPT) systems have attracted considerable attention because WPT systems eliminate the need for cable connections between the charger and the mobility. Therefore, WPT systems have been widely studied for battery charging applications owing to advantages in safety and convenience[1–2].

One of the most critical requirements for battery chargers is achieving rapid charging to reduce charging time. Consequently, WPT systems with a charging capability of several kilowatts are necessary. However, high-power WPT systems tend to be bulky and heavy, which limits an applicability to small mobility. The increased size and weight of the transfer coil make it difficult to apply such high-power systems to compact mobility.

An effective approach to reduce the weight and size of transfer coils is to increase the operating frequency of the WPT system. As the operating frequency increases, the required inductance of the transmitter coil decreases, resulting in reductions in both the size and weight of the transfer coil. Currently, WPT systems operating at 85 kHz are widely adopted, as 85 kHz has been standardized for electric vehicle (EV) chargers. The application of megahertz-band frequencies to WPT systems has been actively investigated[3–7]. Operation in the megahertz range enables the use of air-core coil as the transfer coil, offering a promising solution.

Megahertz-range WPT systems require high-frequency inverters on the transmitter side. Gallium Nitride (GaN) devices are widely adopted in high-frequency inverters to enable high-speed switching at megahertz frequencies. Nevertheless, the output power of each inverter is limited due to the small chip area of GaN devices.

Therefore, parallel connection of GaN devices or inverter circuits is necessary to increase the output current. However, current imbalance tends to occur among the paralleled devices or circuits due to variations in device parameters and differences in switching timing. The current imbalance leads to thermal imbalance, which may damage the devices and associated circuits. Thus, a current balancing method is required to ensure reliable operation of the parallel-connected GaN devices or inverters.

Applying accurate control to synchronize the switching timings of each GaN device or inverter circuit is difficult, since the required control period must be shorter than a few nanoseconds under megahertz-frequency operation. Therefore, current balancing should be achieved without any additional control. Ref.[8] investigated the implementation of parallel-connected GaN devices. Nevertheless, accurate analysis and dedicated circuit design are still required to ensure reliable operation.

Alternatively, current balancers for parallel-connected inverters operating in the megahertz range have been explored to increase output power [9]. Although the reported current balancer consists of two transformers and operates without additional control, the design methodology for the circuit parameters has not been sufficiently discussed.

This paper proposes a current balancer integrated with an impedance-matching circuit for WPT systems. The proposed configuration mitigates parameter constraints on passive components used in the balancing circuit. First, the current balancing mechanism is theoretically analyzed, and an expression for the current imbalance rate is derived. The validity of the derived expression is confirmed through simulation results. Finally, the operation of the proposed current balancer is experimentally demonstrated at 6.78 MHz.

II. Proposed Balancer Circuit

Fig. 1 shows the circuit configuration of the primary side of a WPT system with the proposed current balancer. The

979-8-3315-1886-8/25/$31.00 ©2025 IEEE

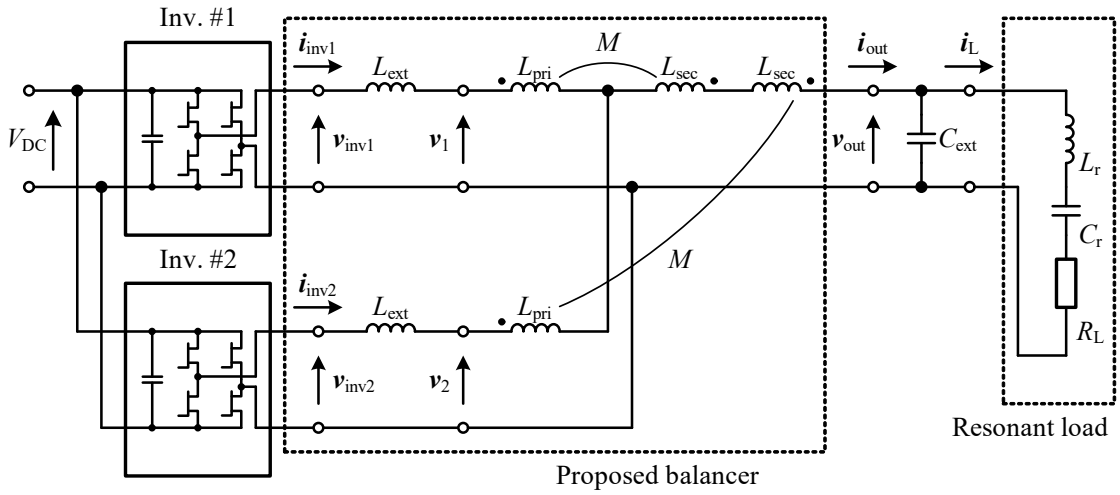


Fig. 1. Configuration of the balance circuit in parallel-connected inverter system.

proposed balancer consists of two external inductors L_{ext} and two transformers. The primary winding of each transformer is connected to an external inductor L_{ext}. The combination of the external inductors and transformers enables current balancing between the inverters. Two inverters(Inv. #1 and Inv. #2) are connected in parallel through the proposed balancer. An external capacitor C_{ext} forms an impedance-matching circuit with the proposed balancer. A resonant load, representing the characteristics of the WPT system, is connected to the output side of the proposed balancer.

Fig. 2 shows representative waveforms of the currents and voltages in the system. Each current is assumed to be a sinusoidal waveform containing only the fundamental component due to the presence of the resonant load. Similarly, the inverter voltages are also assumed to consist solely of fundamental components, which determine the output power. In addition, a phase difference ϕ may occur between the inverter voltages due to variations in device parameters and switching delays. Then, each inverter voltage is expressed as

$$\boldsymbol{v}_{inv1} = V_{rms}\left\{\cos\left(\frac{\phi}{2}\right) + j\sin\left(\frac{\phi}{2}\right)\right\} \quad \text{..... (1)},$$

$$\boldsymbol{v}_{inv2} = V_{rms}\left\{\cos\left(\frac{\phi}{2}\right) - j\sin\left(\frac{\phi}{2}\right)\right\} \quad \text{..... (2)},$$

where V_{rms} denotes the root-mean-square (RMS) value of the inverter voltage. The inverter voltage is considered a square waveform, except during the deadtime. The amplitude of the inverter voltage V_{inv_max} is derived using Fourier series expansion as

$$V_{inv\_max} = \frac{8}{T}\int_{t_d/2}^{T/4} V_{DC}\sin(\omega t)dt = \frac{4V_{DC}}{\pi}\cos(\pi f t_d) \quad \text{..... (3)},$$

where T is the time period of the fundamental component, f is the fundamental frequency, t_d is the deadtime, and V_{DC} is the DC-link voltage. The RMS value of the inverter voltage is expressed as

$$V_{rms} = \frac{2\sqrt{2}}{\pi}V_{DC}\cos(\pi f t_d) \quad \text{..... (4)}.$$

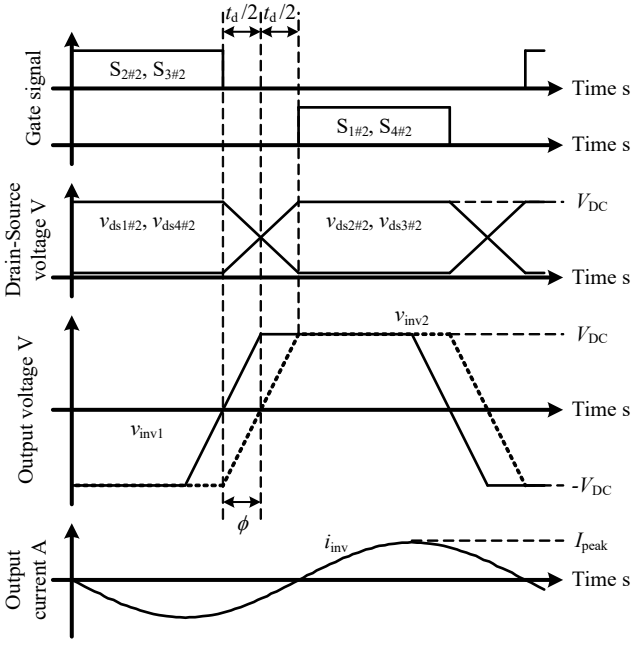


Fig. 2. Representative waveform of each voltage and current.

A. Ideal balance condition

The ideal balancing condition is defined based on the relationship between each inverter current and voltage. The inverter currents $\boldsymbol{i}_{inv1}$ and $\boldsymbol{i}_{inv2}$ have the same amplitude under ideal current balancing. In ideal condition, the phase difference between $\boldsymbol{i}_{inv1}$ and $\boldsymbol{i}_{inv2}$ is zero. The output current $\boldsymbol{i}_{out}$ becomes twice the amplitude of a each input current. Moreover, the output voltage $\boldsymbol{v}_{out}$ is the average of the inverter voltages $\boldsymbol{v}_{inv1}$ and $\boldsymbol{v}_{inv2}$. Thus, the ideal condition is expressed as

$$\boldsymbol{i}_{inv1} = \boldsymbol{i}_{inv2} = \frac{\boldsymbol{i}_{out}}{2} \quad \text{..... (5)},$$

$$\boldsymbol{v}_{out} = \frac{\boldsymbol{v}_1 + \boldsymbol{v}_2}{2} \quad \text{..... (6)}.$$

B. Turn ratio of transformer

The turn ratio of each transformer winding is derived based on the ideal balancing condition of the proposed

balancer. The voltage equations for each transformer are given by

$$\boldsymbol{v}_1 = j\omega\left(L_{\text{pri}} - M\right)\boldsymbol{i}_{\text{inv1}} + j\omega\left(2L_{\text{sec}} - M\right)\boldsymbol{i}_{\text{out}} - j\omega M\boldsymbol{i}_{\text{inv2}} + \boldsymbol{v}_{\text{out}} \quad \text{..... (7)},$$

$$\boldsymbol{v}_2 = j\omega\left(L_{\text{pri}} - M\right)\boldsymbol{i}_{\text{inv2}} + j\omega\left(2L_{\text{sec}} - M\right)\boldsymbol{i}_{\text{out}} - j\omega M\boldsymbol{i}_{\text{inv1}} + \boldsymbol{v}_{\text{out}} \quad \text{..... (8)},$$

$$\boldsymbol{v}_1 + \boldsymbol{v}_2 - 2\boldsymbol{v}_{\text{out}} = j\omega\left(L_{pri} - 2M\right)\left(\boldsymbol{i}_{\text{inv1}} + \boldsymbol{i}_{\text{inv2}}\right) + 2j\omega\left(2L_{\text{sec}} - M\right)\boldsymbol{i}_{\text{out}} \quad \text{..... (9)},$$

where L_{pri} is the self-inductance of the primary winding, L_{sec} is the self-inductance of the secondary winding, and M is the mutual-inductance. Both transformers are assumed to have identical self-inductance and mutual-inductance. Then, the inductance relationship under the ideal balancing condition is expressed as

$$L_{pri} - 4M + 4L_{\text{sec}} = 0 \quad \text{..... (10)},$$

by substituting (5) and (6) into (9). The mutual inductance M is expressed as

$$M = k\sqrt{L_{pri}L_{\text{sec}}} \quad \text{.....(11)},$$

$$k = 1 \quad \text{..... (12)},$$

where k is the coupling factor, which is assumed to be unity under the ideal balancing condition. The relationship between L_{pri} and L_{sec} is obtained using (10), (11), and (12) as

$$L_{pri} = 4L_{\text{sec}} \quad \text{..... (13)}.$$

Thus, the turn ratio of the transformer required to achieve current balancing is derived as

$$\frac{N_1}{N_2} = 2 \quad \text{..... (14)},$$

where N_1 and N_2 are the numbers of winding turns on the primary and secondary sides, respectively.

C. Current imbalance rate

Although the transformer turn ratio is derived under the ideal current balancing condition, the coupling factor k is not equal to unity in practical implementation. In addition, the proposed balancer includes an external inductor L_{ext} to enhance the current balancing effect. Therefore, the actual current imbalance rate should be derived based on voltage equations that include the coupling factor k and the external inductor L_{ext}.

The voltage equations including the external inductor L_{ext} are expressed as

$$\boldsymbol{v}_{\text{inv1}} = j\omega\left(L_{\text{pri}} + L_{\text{ext}} - M\right)\boldsymbol{i}_{\text{inv1}} + j\omega\left(2L_{\text{sec}} - M\right)\boldsymbol{i}_{\text{out}} - j\omega M\boldsymbol{i}_{\text{inv2}} + \boldsymbol{v}_{\text{out}} \quad \text{..... (15)},$$

$$\boldsymbol{v}_{\text{inv2}} = j\omega\left(L_{\text{pri}} + L_{\text{ext}} - M\right)\boldsymbol{i}_{\text{inv2}} + j\omega\left(2L_{\text{sec}} - M\right)\boldsymbol{i}_{\text{out}} - j\omega M\boldsymbol{i}_{\text{inv1}} + \boldsymbol{v}_{\text{out}} \quad \text{..... (16)},$$

$$\boldsymbol{v}_{\text{inv1}} + \boldsymbol{v}_{\text{inv2}} - 2\boldsymbol{v}_{\text{out}} = j\omega\left(L_{\text{pri}} + L_{\text{ext}} - M\right)\left(\boldsymbol{i}_{\text{inv1}} + \boldsymbol{i}_{\text{inv2}}\right) + j2\omega\left(2L_{\text{sec}} - M\right)\boldsymbol{i}_{\text{out}} - j\omega M\left(\boldsymbol{i}_{\text{inv1}} + \boldsymbol{i}_{\text{inv2}}\right) \quad \text{..... (17)}.$$

The output voltage v_{out} is defined as

$$\boldsymbol{v}_{\text{out}} = \left(R_{\text{out}} + jX_{\text{out}}\right)\boldsymbol{i}_{\text{out}} \quad \text{..... (18)},$$

where R_{out} and X_{out} are the real and imaginary parts, respectively, of the output-side impedance. The output current of the proposed balancer i_{out} is derived as

$$\boldsymbol{i}_{\text{out}} = \frac{R_{\text{out}} - j\left(X_{\text{out}} + 4\omega L_{\text{sec}}\left(1-k\right) + \dfrac{\omega L_{\text{ext}}}{2}\right)}{{R_{\text{out}}}^2 + \left(X_{\text{out}} + 4\omega L_{\text{sec}}\left(1-k\right) + \dfrac{\omega L_{\text{ext}}}{2}\right)^2} V_{\text{rms}}\cos\left(\frac{\varphi}{2}\right) \quad \text{..... (19)},$$

by substituting (1), (2), (4), (11), (13), and (18) into (17). Similarly, the inverter currents i_{inv1} and i_{inv2} are derived as

$$\boldsymbol{i}_{\text{inv1}} = \frac{R_{\text{out}} - j\left(X_{\text{out}} + 4\omega L_{\text{sec}}\left(1-k\right) + \dfrac{\omega L_{\text{ext}}}{2}\right)}{2\left\{{R_{\text{out}}}^2 + \left(X_{\text{out}} + 4\omega L_{\text{sec}}\left(1-k\right) + \dfrac{\omega L_{\text{ext}}}{2}\right)^2\right\}} V_{\text{rms}}\cos\left(\frac{\phi}{2}\right) + \frac{1}{4\omega L_{\text{sec}}} \times V_{\text{rms}}\sin\left(\frac{\phi}{2}\right) \quad \text{..... (20)},$$

$$\boldsymbol{i}_{\text{inv2}} = \frac{R_{\text{out}} - j\left(X_{\text{out}} + 4\omega L_{\text{sec}}\left(1-k\right) + \dfrac{\omega L_{\text{ext}}}{2}\right)}{2\left\{{R_{\text{out}}}^2 + \left(X_{\text{out}} + 4\omega L_{\text{sec}}\left(1-k\right) + \dfrac{\omega L_{\text{ext}}}{2}\right)^2\right\}} V_{\text{rms}}\cos\left(\frac{\phi}{2}\right) - \frac{1}{4\omega L_{\text{sec}}} \times V_{\text{rms}}\sin\left(\frac{\phi}{2}\right) \quad \text{..... (21)}.$$

The current imbalance amount is defined as the difference between i_{inv1} and i_{inv2}, and is expressed as

$$\text{Re}\left[\boldsymbol{i}_{\text{inv1}}\right] - \text{Re}\left[\boldsymbol{i}_{\text{inv2}}\right] = \frac{1}{2\omega L_{\text{sec}}} \times V_{\text{rms}}\sin\left(\frac{\phi}{2}\right) \quad \text{..... (22)}.$$

Then, a current imbalance rate a is defined based on the output current i_{out} and the imbalance amount given in (22). The current imbalance rate a is expressed as

$$a = \frac{\dfrac{V_{\text{rms}}}{\omega\left(4L_{\text{sec}} + L_{\text{ext}}\right)}\sin\left(\dfrac{\phi}{2}\right)}{\left|\boldsymbol{i}_{\text{out}}\right|/2} \times 100 = \frac{2\sqrt{{R_{\text{out}}}^2 + \left(X_{\text{out}} + 4\omega L_{\text{sec}}\left(1-k\right) + \dfrac{\omega L_{\text{ext}}}{2}\right)^2}}{\omega\left(4L_{\text{sec}} + L_{\text{ext}}\right)}\left|\tan\left(\frac{\varphi}{2}\right)\right| \times 100 \quad \text{..... (23)}.$$

As a result, the external inductor L_{ext} reduces the current imbalance rate a.

D. Integrated impedance matching circuit

Each inverter requires an appropriate output-side impedance to achieve soft switching. In particular, for a full-bridge inverter circuit, the output current must lag behind the voltage in order to achieve Zero Voltage Switching(ZVS) operation. Although each inverter current should exhibit a phase lag for ZVS, the power factor of the resonant load must be unity due to the transmitter-side characteristics in WPT systems. Thus, impedance matching between each inverter and the resonant load is necessary.

Fig. 3(a) shows the equivalent circuit of the proposed balancer including the output impedance at each inverter. The output impedance of each inverter $\boldsymbol{Z}_{\text{inv}}$ is expressed as

$$\boldsymbol{Z}_{\text{inv}} = r_{\text{inv}} + jx_{\text{inv}} \quad \text{..... (24)},$$

where r_{inv} and x_{inv} are the real and imaginary parts, respectively, of the output impedance required to achieve ZVS. Then, the voltage equations related to the output voltage v_{out} are given by

$$\begin{aligned}&(r_{inv}+jx_{inv})\boldsymbol{i}_{inv1}\\&=j\omega(4L_{sec}+L_{ext})\boldsymbol{i}_{inv1}+2j\omega L_{sec}(1-2k)\boldsymbol{i}_{out}+\boldsymbol{v}_{out}\end{aligned} \quad \text{..... (25),}$$

$$\begin{aligned}&(r_{inv}+jx_{inv})\boldsymbol{i}_{inv2}\\&=j\omega(4L_{sec}+L_{ext})\boldsymbol{i}_{inv2}+2j\omega L_{sec}(1-2k)\boldsymbol{i}_{out}+\boldsymbol{v}_{out}\end{aligned} \quad \text{..... (26).}$$

The impedance relationship at the output of the proposed balancer is obtained by adding (25) and (26), and is expressed as

$$\frac{\boldsymbol{v}_{out}}{\boldsymbol{i}_{out}}=\frac{r_{inv}}{2}+j\left(\frac{x_{inv}}{2}-\omega\left(4L_{sec}(1-k)+\frac{L_{ext}}{2}\right)\right) \quad \text{..... (27).}$$

Fig.3(b) shows the equivalent circuit on the load side of the proposed balancer. The load is modeled as a resistor R_L, since the power factor on the transmitter side of the WPT system is unity at the resonant frequency. The relationship between the output voltage v_{out} and the output current i_{out} is expressed as

$$\frac{\boldsymbol{v}_{out}}{\boldsymbol{i}_{out}}=\frac{R_L}{1+(\omega C_{ext}R_L)^2}-j\left\{\frac{\omega C_{ext}R_L{}^2}{1+(\omega C_{ext}R_L)^2}\right\} \quad \text{..... (28),}$$

Based on (27) and (28), the impedance matching conditions are given by

$$\frac{R_L}{1+(\omega C_{ext}R_L)^2}=\frac{r_{inv}}{2} \quad \text{..... (29),}$$

$$\frac{\omega C_{ext}R_L{}^2}{1+(\omega C_{ext}R_L)^2}=4\omega L_{sec}(1-k)+\frac{\omega L_{ext}}{2}-\frac{x_{inv}}{2} \quad \text{..... (30).}$$

The external capacitance C_{ext} and inductance L_{ext} under the impedance matching condition are derived as

$$C_{ext}=\frac{1}{\omega R_L}\sqrt{\frac{2R_L}{r_{inv}}-1} \quad \text{..... (31),}$$

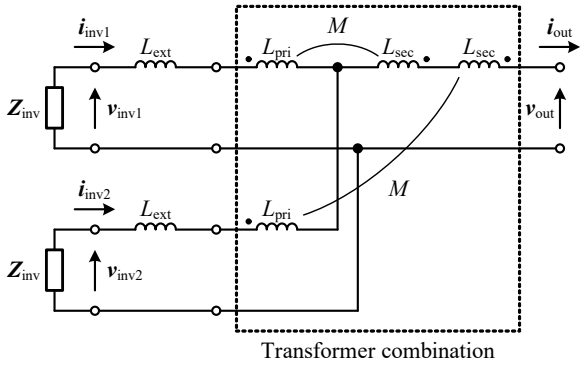
$$L_{ext}=\frac{2C_{ext}R_L{}^2}{1+(\omega C_{ext}R_L)^2}+\frac{x_{inv}}{\omega}-8L_{sec}(1-k) \quad \text{..... (32).}$$

The required value of the external inductor L_{ext} is reduced due to the presence of the transformer, since the leakage inductance is effectively inserted in series with the external inductor.

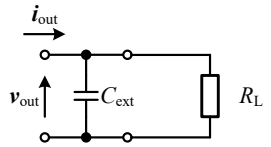
III. Simulation

The current balancing performance of the proposed balancer is evaluated through simulation. Table 1 lists the simulation parameters. The switching frequency is set to 6.78-MHz, which corresponds to that of the target WPT system. The output impedance of each inverter is determined by the output capacitance of the GaN devices in each inverter. The transformer parameters are based on the prototype balancer. The load parameters are calculated based on the resonant frequency, which is equal to the switching frequency. The simulation is conducted using PLECS(Plexim Inc.).

Fig. 4 shows the simulation results under the condition without a voltage phase difference. The load resistance is set to 50 Ω. ZVS is achieved in both inverters. In addition, the amplitude and phase of the inverter currents show good agreement. The output current i_{out} reaches twice the amplitude of each inverter current. Consequently, the output power at the load resistor reaches 6.6 kW.



(a) Input-side configuration with output impedance $\boldsymbol{Z}_{inv}$.



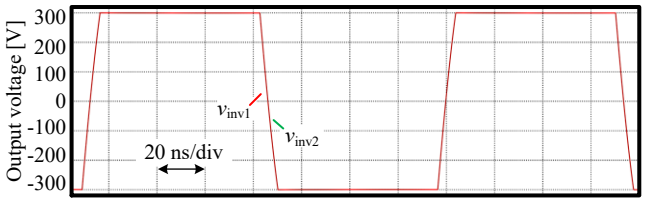
(b) Output-side configuration with load resistance R_L.

Fig. 3. Impedance matching in proposed structure.

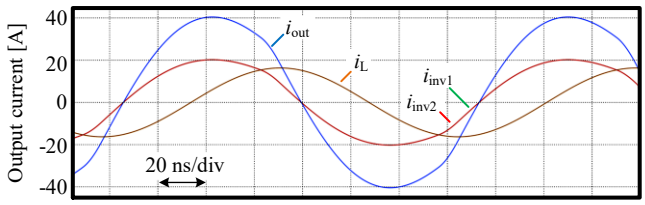
Table 1. Simulation parameter.

Main circuit		
DC link voltage	V_{DC}	300 V
Switching frequency	F_s	6.78 MHz
Duty	d	37.5%
Inverter		
Input reistance of Inverter	r_{inv}	15 Ω
Input leactance of Inverter	x_{inv}	10 Ω
Load		
Resonant inductance	L_r	5.3 μH
Resonant capacitance	C_r	104 pF
Load resistance	R_L	50.0 Ω
Balancer		
Inductance of primary side	L_{pri}	2.2 μH
Inductance of secondary side	L_{sec}	0.55 μH
Coupling factor	k	0.87
Additional inductor	L_{ext}	325 nH
Impedance matching		
Additional capacitor	C_{ext}	2.2 nF

Fig. 5 shows the simulation results with a 100 Ω load resistor. The external capacitor C_{ext} calculated from (31), is 824 pF. The external inductor L_{ext} calculated from (32), is 723-nH. The amplitude and phase of the inverter currents are not affected by the change in load resistance. Moreover, ZVS is

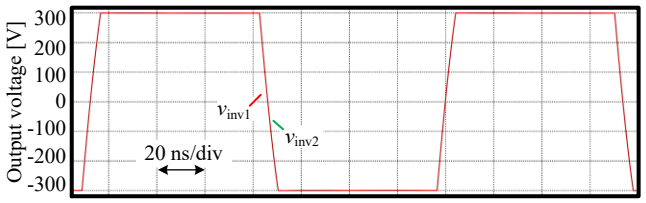


(a) Output voltage.

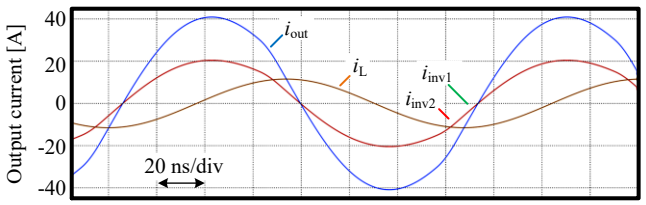


(b) Output current.

Fig. 4. Simulation result without phase delay and impedance matching to 50 Ω load.



(a) Output voltage.



(b) Output current.

Fig. 5. Simulation result without phase delay and impedance matching to 100 Ω load

also achieved in both inverters. Although the amplitude of the load current decreases to approximately 70% (1/1.42) of that in Fig. 4, the output power at the load resistor still reaches 6.6-kW due to effective impedance matching.

Fig. 6 shows the simulation results with a voltage phase difference. The phase of inverter #2 is set to have a 5% delay relative to inverter #1. The load resistance is set to 50 Ω. The inverter current balance is almost maintained even under the condition with a voltage phase difference. The current imbalance rate calculated using (23) is 2.6%, while the rate obtained from the simulation results is 2.2%. Thus, the analytical expression of the current imbalance rate in (23) is validated for the proposed balancer. In addition, ZVS is nearly achieved in both inverters.

IV. Experiment

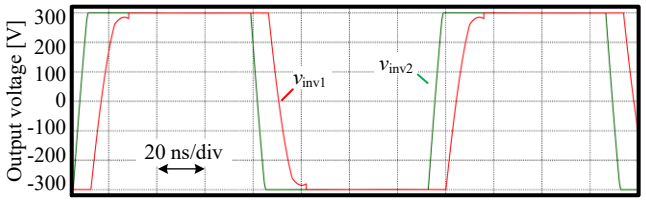
The high-power inverter with parallel operation is evaluated using the prototype balancer at 6.78 MHz. Fig.7 shows the prototype transformer used in the proposed balancer. The primary winding has 8 turns, and the secondary winding has 4 turns. The prototype transformer employs a dust core made of Carbonyl-iron for operation in the megahertz frequency range.

Fig. 8 shows an overview of the experimental setup. The load resistor is cooled by a water-cooled heatsink. The resonant frequency of the load is adjusted to 6.78 MHz, taking into account the water-cooled resistor, resonant inductor, resonant capacitor, and wiring.

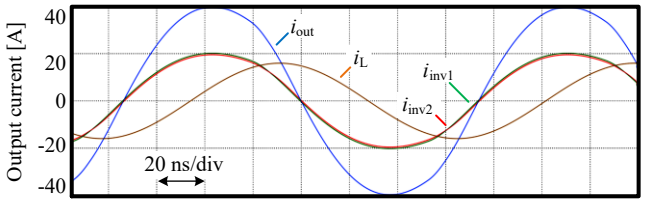
Fig.9 shows the experimental results obtained with the prototype balancer. The DC-link voltage is set to 300 V. The current amplitudes of the inverters are nearly equal, except for low-order harmonic components. One cause of the low-order harmonics is the parasitic capacitance between the primary and secondary windings of the transformer. The output current i_{out} reaches twice the amplitude of each inverter current. Consequently, the input DC power reaches 6.5 kW at 6.78-MHz.

V. Conclusion

This paper proposed a current balancer integrated with an impedance-matching circuit for WPT systems. The proposed balancing circuit was theoretically analyzed, and an expression for the current imbalance rate was derived.



(a) Output voltage.



(b) Output current.

Fig. 6. Simulation result with 5% phase delay and impedance matching to 50 Ω load

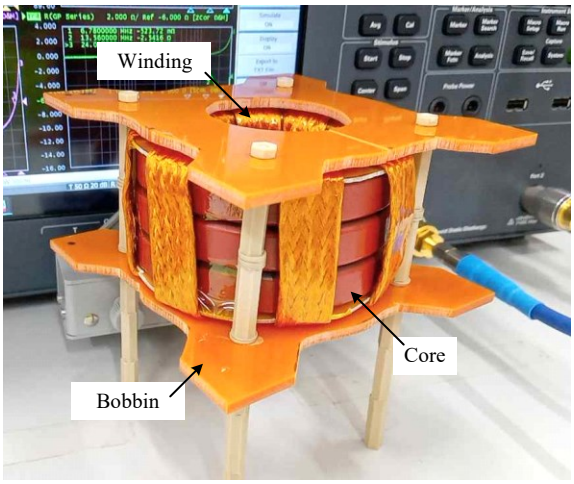


Fig. 7. Simulation result with 5% phase delay and impedance matching to 50 Ω load

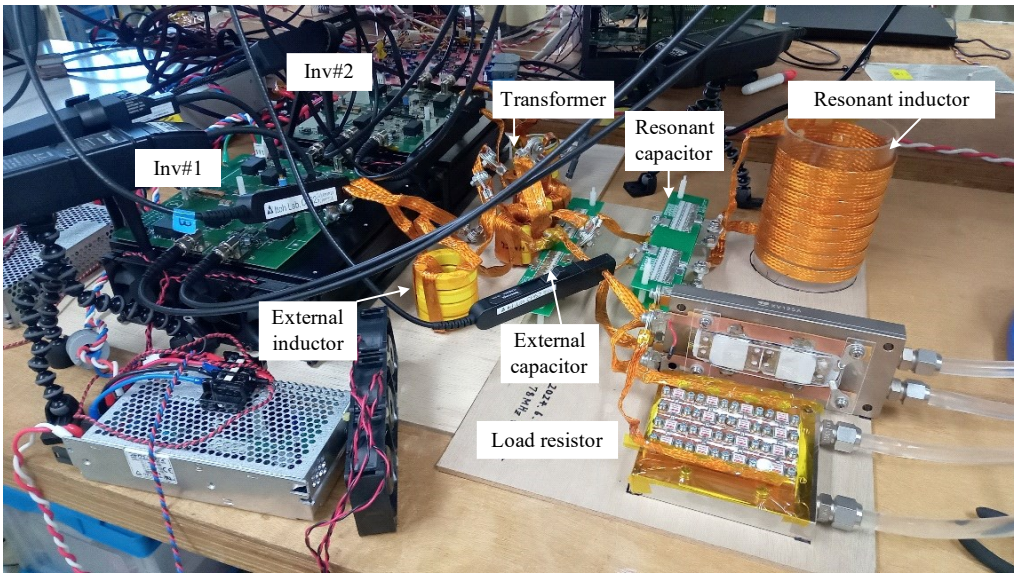


Fig. 8. Experimental waveform with V_{DC}:300 V.

Simulation results validated the operation of the proposed balancer, with the simulated imbalance rate closely matching the theoretical value an error of only 0.2 percentage points. Additionally, combining the proposed balancer with an external capacitor successfully achieved impedance matching between each inverter and the load. ZVS operation was achieved under varying load resistances by adjusting the matching parameters. The effectiveness of the proposed balancer was further confirmed through experiments using a prototype. Both impedance matching and ZVS operation were demonstrated in the experimental setup. Finally, the prototype balancer enabled an output power of over 6 kW at 6.78 MHz.

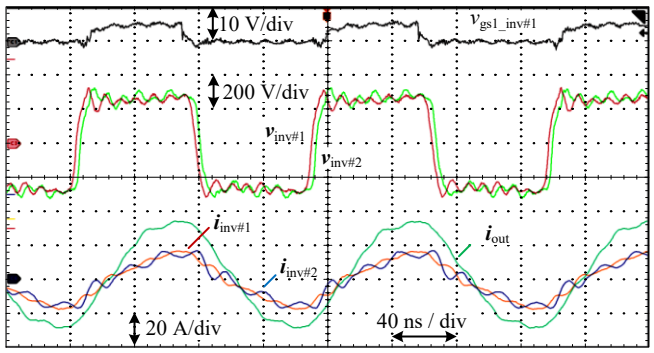


Fig. 9. Experimental waveform with V_{DC}:300 V.

REFERENCES

[1] N. K. Trung, T. Ogata, S. Tanaka, K. Akatsu, “Analysis and PCB Design of Class D Inverter for Wireless Power Transfer Systems Operating at 13.56MHz”, IEEJ Journal of Industry Applications, 2015, vol 4, no.6, pp. 703-713.

[2] S. Suzuki, T. Shimizu, “A Study on Efficiency Improvement of High-frequency Current Output Inverter Based on Immittance Conversion Element”, IEEJ Journal of Industry Applications, 2015, vol 4, no.3, pp. 220-226.

[3] M. Fu, Z. Tang and C. Ma, "Analysis and Optimized Design of Compensation Capacitors for a Megahertz WPT System Using Full-Bridge Rectifier," in IEEE Transactions on Industrial Informatics, vol. 15, no. 1, pp. 95-104, Jan. 2019, doi: 10.1109/TII.2018.2833209.

[4] M. Liu, M. Fu, Y. Wang and C. Ma, "Battery Cell Equalization via Megahertz Multiple-Receiver Wireless Power Transfer," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 4135-4144, May 2018, doi: 10.1109/TPEL.2017.2713407.

[5] J. Song, M. Liu and C. Ma, "Efficiency optimization and power distribution design of a megahertz multi-receiver wireless power transfer system," 2017 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW), Chongqing, China, 2017, pp. 54-58, doi: 10.1109/WoW.2017.7959364.

[6] M. Fu, H. Yin and C. Ma, "Megahertz Multiple-Receiver Wireless Power Transfer Systems With Power Flow Management and Maximum Efficiency Point Tracking," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 11, pp. 4285-4293, Nov. 2017, doi: 10.1109/TMTT.2017.2689747.

[7] J. Shi, L. Zhou and X. He, "Common-Duty-Ratio Control of Input-Parallel Output-Parallel (IPOP) Connected DC–DC Converter Modules With Automatic Sharing of Currents," in IEEE Transactions on Power Electronics, vol. 27, no. 7, pp. 3277-3291, July 2012, doi: 10.1109/TPEL.2011.2180541.

[8] N. K. Trung and K. Akatsu, "Design challenges for 13.56MHz 10 kW resonant inverter for wireless power transfer systems", 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019, pp. 1-7.

[9] M. Yamaguchi, K. Kusaka and J. Itoh, "Current Balancing Method in Parallel Connected Inverter Circuit for Megahertz WPT System," 2021 IEEE 30th International Symposium on Industrial Electronics (ISIE), 2021, pp. 1-6, doi: 10.1109/ISIE45552.2021.9576365