High-Frequency Current-Doubler Rectifier-Based Buck Capacitive-Isolated Converter

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***Abstract*— This paper proposes a buck-type capacitive isolated DC–DC converter without a magnetic transformer. The proposed topology operates as a current-doubler rectifier (CDR) to achieve a high step-down ratio for low DC voltage applications. A design method for the isolation capacitance and output inductance is also presented to achieve MHz operation. The experimental results show the steady-state operation of the proposed converter. Moreover, a maximum efficiency of 89.7% was confirmed with 1 MHz switching frequency.**

Keywords*— *Capacitive isolation, current-doubler rectifier, high-frequency power conversion

I. INTRODUCTION

In recent years, isolated DC–DC converters have been widely used in applications such as rapid chargers [1]–[3] and onboard chargers (OBCs) [4]–[8]. In conventional isolated DC–DC converters, electrical isolation between the primary and secondary sides is typically achieved using a magnetic isolation transformer. However, a magnetic transformer may limit the miniaturization of the power converters. On the other hand, the capacitive isolation has been investigated as a promising alternative that enables a significant reduction in converter volume [9]–[11].

A capacitive-isolated converter based on an LLC-type resonant cell is presented in [9]. By replacing the magnetic transformer with isolation capacitors, the converter reduces the magnetic volume while maintaining soft switching through the LLC resonant network. Since the operating point is constrained around the resonant frequency and the resonant current decreases with load, the soft-switching operation becomes sensitive to load variation. Another capacitive-isolation approach is reported in [10], where high efficiency is achieved without magnetic components by utilizing a resonant switched-capacitor configuration. Although this method effectively suppresses high-frequency common-mode current, its soft-switching transitions depend on the resonant current. When the resonant current decreases under load variation, the ZVS condition cannot be maintained, and the switching frequency must be adjusted accordingly. This reliance on load-dependent resonant current is a fundamental limitation of the approach. In resonant-type capacitive-isolation converters, the inductor current is dominated by the resonant-frequency component, which increases the RMS current and the magnetic loss. This behavior limits the extent to which the inductor can be reduced in size compared with non-resonant capacitive-isolation converters.

A capacitive-isolated converter derived from the dual-active bridge is presented in [11]. In this topology, the transformer is replaced with isolation capacitors while the converter retains the same SPS switching behavior as a conventional DAB. Since the inductor current is determined by the switching-frequency operation rather than by resonance, high-frequency current still dominates the inductor waveform. As a result, the converter faces the same fundamental limitation regarding inductor reduction as resonant-type capacitive-isolation converters.

This paper proposes a current-doubler rectifier (CDR)-based buck capacitive-isolated converter. In contrast to resonant-type capacitive-isolation converters and DAB-derived capacitive-isolation converters, the proposed topology does not generate an inductor current dominated by a high-frequency component, thus it does not impose the same limitation on inductor miniaturization. The proposed converter is designed for automotive auxiliary power systems that require a compact, high-step-down topology. The proposed converter has a step-down ratio of 0.25 by combining a primary-side half-bridge with a secondary-side CDR, enabling a high step-down ratio

even in a transformerless configuration. In the proposed CDR-type converter, the secondary-side CDR improves the input–output current ratio to reduce the conduction loss. Furthermore, the switching frequency of the proposed converter is designed above MHz to reduces the isolation capacitance and output inductance. Isolation capacitors have to withstand high-voltage stress. It is important to increase the switching frequency to accept the low capacitance and high voltage rating capacitors.

In this paper, the detail of the operation principle for the proposed converter is introduced. In addition that, some experimental results with the switching frequency of 1 MHz and 1.5 MHz are demonstrated to show the fundamental operation of the proposed converter. Finally, the conversion efficiency of the proposed converter is evaluated based on the converter loss analysis.

II. PROPOSED CONVERTER

Fig. 1 shows the circuit diagram of the proposed CDR-based buck capacitive-isolated converter. The proposed converter consists of a half-bridge converter on the primary side and a CDR on the secondary side, connected via isolation capacitors. The combination of the half-bridge converter and the CDR achieves a step-down operation without a magnetic transformer. The half-bridge converter operates with complementary switching at a 0.5 duty ratio on the upper and lower arms. Note that the duty ratio is varied from 0.5, the input-output voltage gain decreases, and the loss imbalance increases. Thus, this paper examines only the case where the duty ratio is 0.5.

Fig. 2 shows the operation modes of the proposed converter. The operation mode of the proposed converter is defined as mode 1 and mode 2. In mode 1, the output power is delivered from the power supply to the load. In the current path of mode 1, the DC output current is split by the output inductors L_1 and L_2, and the isolation capacitors C_1 and C_2 are charged by the inductor current i_{L1}. In addition, L_1 is charged by the power supply, while L_2 is discharged according to the DC output voltage. In Mode 2, the output power is delivered from the isolation capacitors to the load. In the current path of Mode 2, similar to Mode 1, the DC output current is split by the output inductors, and the isolation capacitors are discharged by the inductor current i_{L2}. In addition, L_2 is charged by the isolation capacitor, while L_1 is discharged according to the DC output voltage.

The transition between Mode 1 and Mode 2 causes the isolation-capacitor currents i_{C1} and i_{C2} to reverse its direction. Meanwhile, the direction of the output-inductor current i_{L1} and i_{L2} remains unchanged because the output-inductor current ripple Δi_L is designed to be smaller than the DC output current I_{out}. As a result, the isolation-capacitor current forms a square-wave shape, while the output-inductor current is dominated by its DC component. This characteristic reduces the high-frequency current flowing through the output inductors, thereby mitigating the limitation on inductor miniaturization caused by high-frequency losses. Furthermore, in each mode, the output inductors charge and discharge in a complementary manner, and their charge/discharge currents cancel each other. This reduces the output-current ripple and enables downsizing of the output capacitor.

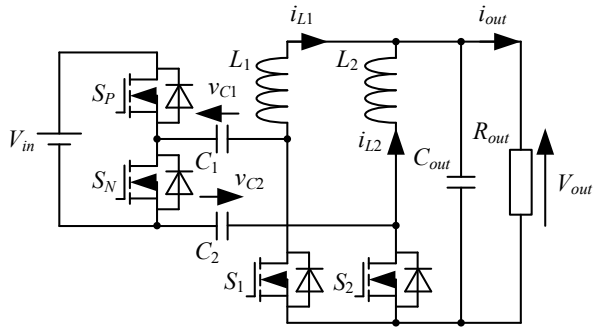
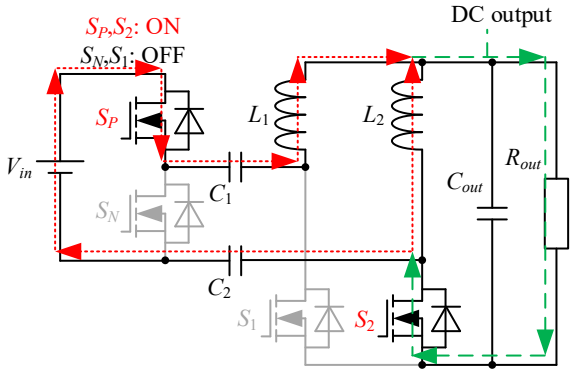
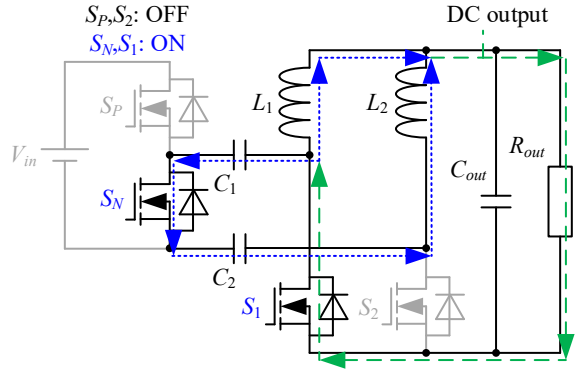


Fig. 1. Circuit configuration of buck capacitive isolation converter with current-doubler-rectifier.



(a) Mode 1: S_P and S_2 are turned ON, while S_N and S_1 are turned OFF.



(b) Mode 2: S_P and S_2 are turned OFF, while S_N and S_1 are turned ON.

Fig. 2. Operating mode diagrams of the proposed circuit based on switch states.

Fig. 3 shows the isolation capacitor voltage, isolation capacitor current, output-inductor voltage, and output-inductor current waveforms during operation of the proposed converter. In Fig. 3, the output-inductor current remains in the forward direction without zero-crossing, provided that the output-inductor current ripple is designed to be smaller than the DC output current, so the DC component becomes dominant. Note that the operation behavior during the dead time does not considered.

According to Fig. 3, the isolation capacitors are charged during Mode 1 and discharged during Mode 2. The isolation-capacitor currents i_{C1} and i_{C2} take a square-wave shape, so the isolation-capacitor voltages v_{C1} and v_{C2} become triangular. Since the input power supply charges the isolation capacitors, their

charging/discharging is limited to the input voltage range of V_{in}. During charging/discharging, the two isolation capacitors C_1 and C_2 are connected in series, so the maximum isolation capacitor voltage ripple Δv_C is $V_{in}/2$. Once the isolation-capacitor voltage reaches its upper limit, the charging process is limited in Mode 1. Similarly, once it reaches its lower limit, the discharging process is limited in Mode 2. These limitations restrict the achievable output power in both modes. Consequently, the input-output voltage gain of the proposed converter decreases from 0.25 as the load size increases. In this paper, to avoid degradation of the input-output voltage gain, the isolation capacitance is designed to prevent voltage saturation across the isolation capacitors. The isolation capacitor currents i_{C1} and i_{C2} are equal to the output-inductor current i_{L1} in Mode 1 and equal to i_{L2} in Mode 2. Here, approximating that the average value of the output-inductor current equals half the DC output current I_{out}, the condition preventing saturation of the isolation capacitor voltage can be expressed as in (1),

$$C \geq \frac{P_{rated}}{2 f_{SW} V_{out} V_{in}} \quad \text{.....(1),}$$

where C is the isolation capacitance, a which is designed such that $C=C_1=C_2$, Vin is the input voltage, V_{out} is the output voltage, P_{rated} is the rated power and f_{sw} is the switching frequency. The value of C is determined based on the designed voltage ripple Δv_C across the isolation capacitors, which must be chosen so that it remains within the voltage limits of 0 and $V_{in}/2$ established by the primary-side half-bridge. The capacitance C is calculated as

$$C = \frac{P_{rated}}{4 f_{SW} V_{out} \Delta v_C} \quad \text{.....(2).}$$

According to (2), it is desirable to set Δv_C relatively large to facilitate converter miniaturization.

From the output-inductor voltages v_{L1} and v_{L2} and the inductor currents i_{L1} and i_{L2} shown in Fig. 3, the operation of output inductors L_1 and L_2 is complementary in Mode 1 and Mode 2, respectively. In this paper, the output inductance is designed based on the output-inductor current ripple Δi_L. Focusing on v_{L1} and i_{L1} in Mode 2, the output inductance can be designed as in (3),

$$L = \frac{V_{out}}{2 f_{SW} \Delta i_L} \quad \text{.....(3),}$$

where L is the output inductance, which is designed such that $L=L_1=L_2$. However, if the isolation capacitor voltage ripple Δv_C exceeds $V_{in}/4$, the output-inductor voltage crosses zero during the mode transition, causing a peak in the output-inductor current. Consequently, the output-inductor current ripple becomes larger than that calculated from (3). Furthermore, since the proposed converter is designed to operate under the condition that the resonant frequency is determined by the isolation capacitor and the output-inductor is kept well below the switching frequency, the converter must satisfy this condition, and the output inductance L must satisfy the condition given in (4),

$$f_{SW} \gg \frac{1}{2\pi\sqrt{LC}} \quad \text{.....(4).}$$

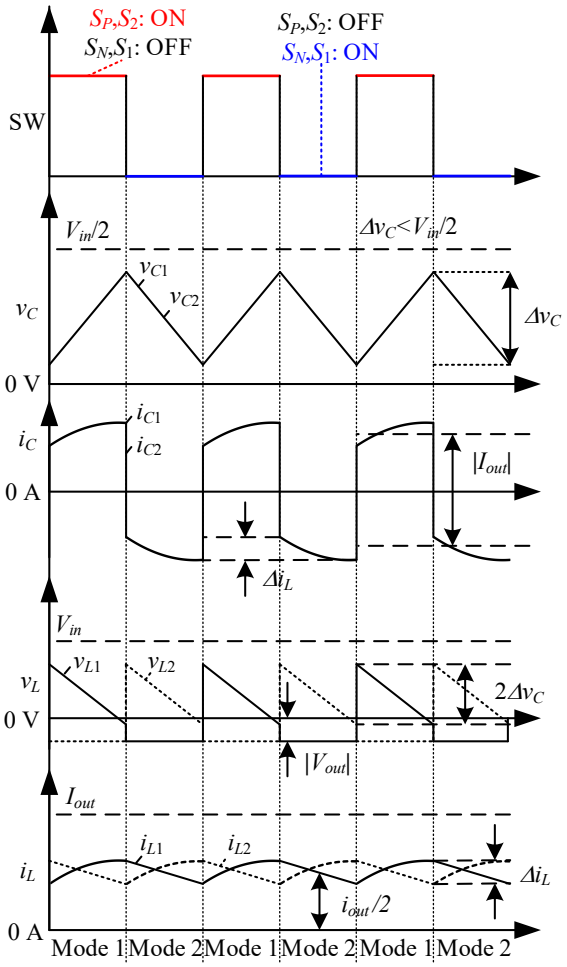


Fig. 3. Voltage and current waveforms of isolation capacitor and output inductor.

III. EXPERIMENTAL RESULTS

Table 1 shows the circuit parameters used in the experimental verification and the part numbers used in the prototype. In this paper, the converter was operated at switching frequencies of 1 MHz and 1.5 MHz to verify proper operation and to measure its efficiency characteristics. The circuit parameters were designed for a switching frequency of 1 MHz, and the isolation capacitances and output inductances were used without modification at 1.5 MHz. The output voltage was fixed at 12 V, and the input voltage was varied with the output power and switching frequency during the experiments. Loss estimation was performed by obtaining component characteristics from the datasheets listed in Table 2. Furthermore, the isolation capacitor was designed with an isolation withstand voltage of 2.5 kV, comprising 20 capacitors arranged in 4 in series and 5 in parallel.

A. Circuit Operation Verification

Fig. 4 shows the operating waveforms of the proposed converter at rated power output. Fig. 4(a) shows the waveforms at a switching frequency of 1 MHz and an output power of 0.97 p.u. Calculating the isolation capacitor voltage ripple at 0.97 p.u. using (2) gives 19.5 V_{pp}. The experimentally measured value

was 18 V_{pp}, a difference of -7.7% from the theoretical value. The output-inductor current ripple was set to 0.5 A. The experimentally measured value was 0.62 App, a 24% difference from the theoretical value. Similarly, comparisons with theoretical values are made for the switching frequency of 1.5 MHz and output power of 1.0 p.u. shown in Fig. 4(b). From (2), the voltage ripple across the isolation capacitor at 1.5 MHz is 13.3 V_{pp}. The experimentally measured value was 12 V_{pp}, resulting in a difference of -9.8% from the theoretical value. From (3), the output current ripple at 1.5 MHz is 0.33 A_{pp}. The experimentally measured value was 0.43 A_{pp}, showing a 30.3% deviation from the theoretical value. The error of the isolation capacitor voltage ripple is primarily due to dead time. Dead time reduces the charge/discharge time of the isolation capacitor, resulting in a measured value in the actual device that is smaller than the design value. Furthermore, the error factors for the output-inductor current ripple are assumed to be the reduction in the input-to-output voltage gain due to dead time and resistive components. In the experiment, the input voltage was increased from the design conditions to achieve a constant output voltage. Since the output-inductor voltage is affected by the input voltage, it is presumed that the output-inductor current ripple increased as the input voltage rose.

B. Input/Output Voltage Characteristics

Fig. 5 shows the input-output voltage characteristics of the converter at a switching frequency of 1 MHz. In the ideal case, the input-output voltage gain of the proposed converter is 0.25. However, in practice, the output voltage is reduced by dead time, the ESR of the isolation capacitors, the on-resistance of the switching devices, and the winding resistance of the output inductors. Thus, when performing loss analysis based on simulations under ideal conditions, discrepancies with actual operating conditions may become significant, potentially challenging loss estimation. To reproduce the experimental behavior, a simulation was performed that accounted for dead time, the ESR of the isolation capacitors, the DC resistance of the output inductors, the on-resistance and reverse conduction voltage of the switching devices. The simulation results showed a higher output voltage than the experimental results, closer to the ideal value. When a voltage-drop resistor was added at the DC output in the simulation, the resulting input-output voltage characteristics agreed closely with the experimental results.

C. Loss characteristics

Fig. 6 shows the efficiency characteristics of the proposed converter obtained from the experimental verification. At a switching frequency of 1 MHz, the efficiency reaches 89.7% at an output power of 0.75 p.u. Whereas at 1.5 MHz, it is 86.8% at an output power of 1.0p.u. These experimental results are compared with the loss estimates obtained from simulation.

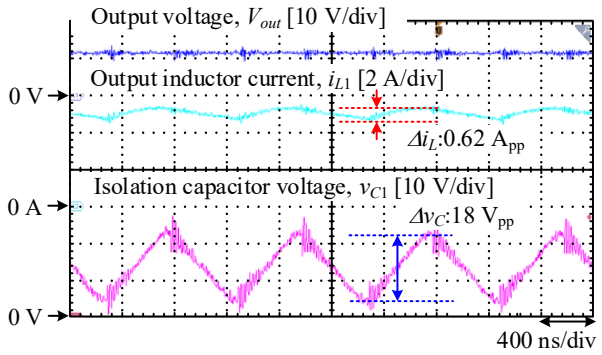
IV. Loss Estimation for the Proposed Converter

The converter losses in the proposed converter are analyzed. The total estimated losses were compared with those obtained from experimental results. A circuit simulator was used to estimate losses by calculating them from the simulation results.

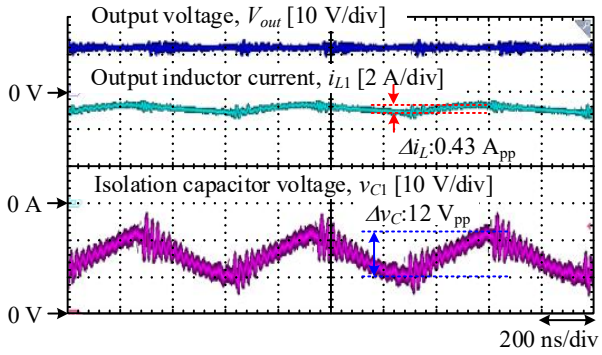
The losses in switching devices are estimated for switching losses and conduction losses. Since GaN devices are used as the switching devices in this paper, the E_{oss} characteristics from the datasheet are used as switching losses. For conduction losses, the drain-source voltage characteristics and reverse conduction characteristics during diode operation are obtained from the datasheet and utilized. A thermal model is created from the characteristics obtained from the datasheet and estimated through simulation.

Table 1. Circuit parameter and manufacturer part number of elements with experiment.

Parameter	Symbol	Value
Output voltage	V_{out}	12 V
Rated power	P_{rated}	120 W
Isolation capacitance	C_1, C_2	125 nF
Output inductance	L_1, L_2	12 µH
Output capacitance	C_{out}	1.5 µF
Switching frequency	f_{SW}	1 MHz 1.5 MHz
Dead-time	T_{dead}	20 ns
Isolation capacitor voltage ripple	Δv_C	20 V_{pp} (1 MHz)
Output inductance current ripple	Δi_L	0.5 A_{pp} (1 MHz)
LC resonance frequency	f_r	130 kHz
Element	**Manufacturer part number**	
Switching devices	EPC2306	
Isolation capacitor	C5750C0G2J104J280KC	
Output inductor core	T94-2	
Output capacitor	C2012X5R1H225K125AB	



(a) f_{SW}: 1 MHz, P_{out} : 0.97p.u.



(b) f_{SW}: 1.5 MHz, P_{out} : 1.0p.u.

Fig. 4. Operational waveforms of the proposed circuit.

Isolation capacitor losses are estimated by performing harmonic analysis on the simulated current waveform using FFT. Isolation capacitor losses are estimated using the ESR characteristics from the datasheet. Since the isolation capacitor current is a square waveform as shown in Fig. 3, losses are calculated for the fundamental wave at the switching frequency and for odd-order harmonic components up to the 11th order.

Output-inductor losses are estimated by performing harmonic analysis on the simulated current waveform using FFT for conduction losses. The DC resistance of the output-inductor's winding resistance is measured using an LCR meter, while the resistance at the switching frequency is measured using a network analyzer. Since the output inductor current is triangular-wave-shaped as shown in Fig. 3, losses are calculated for harmonic components from the fundamental waveform to the fifth harmonic at the switching frequency.

A. Converter loss comparison

Fig. 7 shows the total loss characteristics as a function of output power. A comparison of the experimental and estimated results shows a significant discrepancy between the measured and estimated losses. Furthermore, the slope of the loss variation with respect to output power is larger in the experimental results. However, because the difference between the experimental and estimated results remains relatively consistent across switching frequencies of 1 MHz and 1.5 MHz, it can be inferred that the losses that vary significantly with switching frequency are appropriately accounted for in the loss estimation.

Fig. 8 presents a comparison between the measured losses from experimental verification and the estimated losses for the isolation capacitor, output inductor, and switching devices. Among the estimated losses, switching device losses are the largest, whereas isolation capacitor losses are considerably smaller than those of the other loss components. Furthermore, a comparison of the loss estimation results at 1 MHz and 1.5 MHz shows that the estimation accuracy is about the same for both frequencies. This similarity suggests that the factors contributing to the difference between the estimated and experimental values may be the same. Additionally, the comparisons shown in Figs 5, 7, and 8 indicate that the discrepancy between the experimental and estimated results is attributable to the DC resistance characteristics. Thus, in loss estimation for the proposed converter, it is essential to account for loss factors whose magnitudes vary with the DC components and output power.

B. Switching-device losses estimation

Fig. 9 shows the switching-device losses characteristics at rated power output for the estimated switching frequency of 1 MHz. Here, D_P and D_1 represent losses due to the reverse-conduction characteristics of the switching devices S_P and S_1, respectively. The losses for S_N and S_2 are omitted, as they are assumed to be equal to those of S_P and S_1, respectively. In the half-bridge converter, losses due to E_{oss} dominate because the input current is small compared to the output current and the switching frequency is high. On the CDR side, however, reverse conduction losses during diode operation are larger than those during synchronous rectification. Particularly under conditions where dead-time effects become significant, such as when

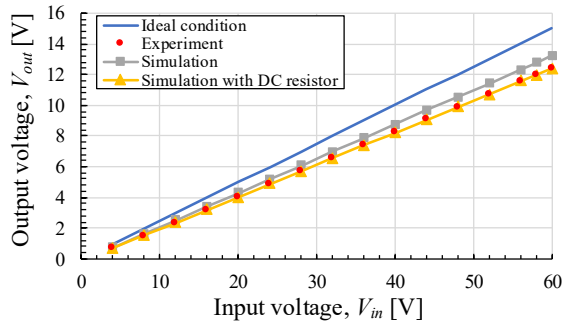


Fig. 5. Output/Input voltage gain characteristics.

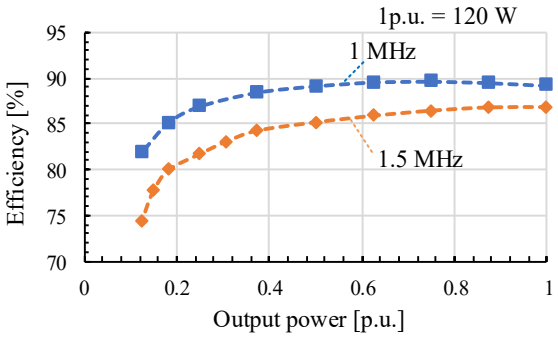


Fig. 6. Efficiency characteristics.

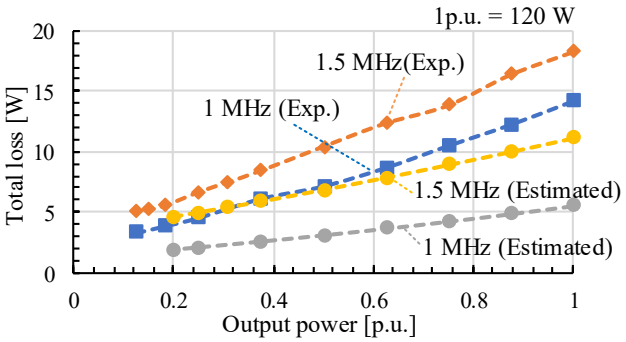


Fig. 7. Total loss characteristics.

increasing the switching frequency, reverse conduction losses on the CDR side become dominant. This could pose a problem for achieving high power density in the converter through high-frequency operation.

V. Conclusions and Future Work

In this paper, a CDR-based buck capacitive-isolated DC–DC converter that eliminates the need for a transformer was developed and evaluated for MHz-class operation. Its efficiency and loss characteristics were evaluated experimentally using a 1-MHz hardware prototype. At a switching frequency of 1 MHz, the proposed converter achieved a maximum efficiency of 89.7%, confirming the practical feasibility of capacitive isolation for high-frequency operation. A comparison between measured and simulated losses clarified the influence of dead time, ESR, and resistive components, providing insight into the dominant loss mechanisms of the proposed topology. Furthermore, the experimental results demonstrated that the isolation capacitor voltage ripple and the output-inductor current ripple closely follow the theoretical trends predicted by (2) and (3), confirming the validity of the proposed design methodology.

Future work will focus on improving the accuracy of the loss analysis, including estimating snubber losses in the DC path and switching losses, and on optimizing circuit parameters for higher-frequency operation and increased power density.

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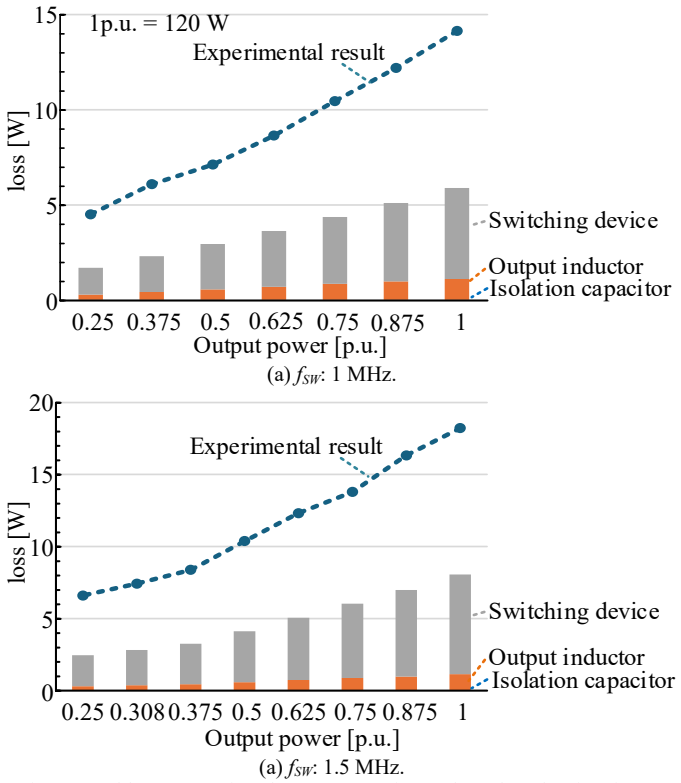

Fig. 8. Total loss comparison between experimental result and estimation.

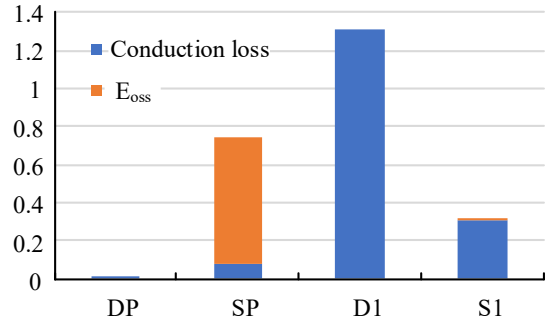

Fig. 9. Loss characteristics of switching devices operating at a switching frequency of 1 MHz under rated power output conditions.