Active Power Decoupling with Capacitor Voltage Utilization Factor Design for Single-phase and Three-phase Compatible T-type Converter in EV On-board Chargers

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***Abstract*— This paper proposes a volume minimization design method for the capacitor voltage utilization factor α in a single-phase and three-phase compatible T-type converter with active power decoupling (APD). The proposed method determines α by quantitatively analyzing the trade-offs between three critical components: the *LCL* filter, the heat sink, and the DC-side capacitors. The *LCL* filter is designed based on a harmonic theoretical equation that accounts for DC-side capacitor voltage fluctuations in order to satisfy grid current THD and reactive power constraints. The experimental results demonstrate that the proposed APD method reduces the second-order harmonic component of the DC voltage by 99.5% at 3.0 kW. In addition, the proposed system achieves a maximum efficiency of 96.8% with a grid current THD of 0.9%. These results validate the effectiveness of the proposed volume minimization method.**

Keywords*— *active power decoupling, on-board charger, single-phase and three-phase compatible, T-type converter

I. INTRODUCTION

In recent years, on-board chargers (OBCs) for electric vehicles have been actively researched [1]-[2]. The OBC must support multiple charging standards and bidirectional power transfer for battery systems to be effectively connected into the AC power grid. In addition, OBCs must be compact to maximize interior space. In response to these requirements, several circuit topologies and control methods focusing on single-phase and three-phase compatibility have been proposed [3]-[4]. When an OBC is connected to a single-phase grid, the instantaneous power on the AC-side pulsates, whereas the DC-side is required to maintain constant power due to the connected battery. Electrolytic capacitors are commonly used on the DC-side in order to absorb power pulsations. However, electrolytic capacitors suffer from thermal degradation according to the Arrhenius law, thereby limiting the lifespan of power converters.

To address this issue, active power decoupling (APD) methods have been proposed [5]-[8]. These methods enable the use of capacitors with smaller capacitance, thereby allowing electrolytic capacitors to be replaced with film capacitors or ceramic capacitors. Several APD methods focusing on single-phase and three-phase compatibility have also been proposed [9]-[11]. Ref. [9] proposes a circuit configuration consisting of an interleaved totem-pole power factor correction (PFC) converter compatible with single-phase and three-phase operation, and an auxiliary buck-type APD circuit. In this approach, the buffer capacitor voltage must be maintained below the DC voltage, which is a disadvantage in terms of minimizing capacitor size. Additionally, this topology requires additional inductors and switching devices. Ref. [10] presents an APD method based on an interleaved totem-pole PFC converter, where the built-in leg in three-phase operation is used as a half-bridge APD circuit. This approach eliminates the need for an additional APD circuit. However, DC voltage pulsations remain due to interference between PFC control and neutral point current control. Ref. [11] introduces another APD method using the *LCL* filter of a three-phase PWM rectifier, which also avoids an additional circuit. Nevertheless, the power factor and total harmonic distortion (THD) of the grid current significantly deteriorate because the AC-side filter capacitor is repurposed for APD.

To address these problems, the authors have proposed a single-phase and three-phase compatible T-type converter with APD capability [12]. The proposed circuit configuration allows independent regulation of the neutral point current and grid current. As a result, residual DC voltage pulsation and power factor degradation, which are observed in Refs. [10] and [11], are effectively suppressed. Moreover, by employing the bidirectional switch in the T-type converter for three-level modulation, the proposed method enables miniaturization of the AC-side filter. However, in this topology, the DC-side capacitor voltage intentionally fluctuates at the grid frequency for APD operation. This introduces a design trade-off between the capacitor voltage amplitude and the resulting harmonic components in the converter output voltage. Consequently, the capacitor voltage utilization factor, which is defined as the ratio between fluctuation voltage and half of the DC voltage, significantly affects not only the DC-side capacitor size but also the required filter size and switching losses. Therefore, it is necessary to determine the capacitor voltage utilization factor based on a comprehensive design approach considering these trade-offs.

This paper proposes a volume minimization design method for the capacitor voltage utilization factor in a single-phase and three-phase compatible T-type converter. The proposed design method determines the capacitor voltage utilization factor such that the following components are minimized:

1. *LCL* filter achieving the desired THD and reactive power ratio
2. Heat sink that maintains junction temperature below a set value during worst-case losses in single-phase operation or three-phase operation.

3. DC-side capacitors corresponding to the capacitor voltage utilization factor.

The *LCL* filter is precisely designed to achieve a desired THD based on the harmonic theoretical equation for converter output voltage, which considers voltage fluctuations of the DC-side capacitor. In addition, the losses caused by switching devices are calculated using a theoretical equation that considers DC-side capacitor voltage fluctuations. The system designed based on the proposed design method is validated by experimental results. The experimental results show that the THD of the grid current is 0.9%. In addition, the maximum efficiency when applying the APD method is 96.8% at 2.5 kW. Additionally, the APD method reduces the second-order harmonic component of the DC voltage by 99.5%.

II. Single-phase and Three-phase Compatible T-type Converter

A. Circuit Configuration

Fig. 1 shows the circuit configuration of the single-phase and three-phase compatible T-type converter. In three-phase operation, the AC grid is connected to terminals T_u, T_v, and T_w, as shown in Fig. 1(a). The mechanical relays R_u and R_v contact the *LCL* filter section when a three-phase grid is connected to each terminal. The mechanical relays R_w and R_n for the w-phase and the *LCL* filter section are changeover contact relays. These relays contact the *LCL* filter section in three-phase operation. Consequently, the circuit functions as a three-phase T-type converter in three-phase operation.

In single-phase operation, the AC grid is connected to terminals T_u and T_v, as shown in Fig. 1(b). The mechanical relays R_u and R_v connect to the *LCL* filter section when the single-phase grid is connected to terminals T_u and T_v, similar to three-phase operation. The w-phase mechanical relay R_w is connected to terminal T_{fw} on the L_f side of the *LCL* filter section. In addition, the mechanical relay R_n of the *LCL* filter section is connected to the neutral point of the DC-side capacitor. As a result, the circuit functions as a single-phase T-type converter and a half-bridge APD circuit during single-phase operation.

Fig. 2 shows the circuit diagram separating the T-type converter side and the APD circuit side in single-phase operation. This circuit configuration achieves APD without additional switching devices and magnetic components in single-phase operation by adding a changeover contact relay to the *LCL* filter section. Furthermore, the two circuit configurations are separated in single-phase operation, which achieves independent control of each circuit.

B. Active Power Decoupling

Fig. 3 shows the principle of active power decoupling. In the single-phase and three-phase compatible T-type converter, DC-side capacitors C_1 and C_2 function as energy buffers for the APD function. Assuming the single-phase grid operates at unity power factor, the instantaneous power on the AC-side, p_{in} is expressed as

$$p_{in} = v_g i_g = V_g I_g - V_g I_g \cos(2\omega_g t) \tag{1}$$

where v_g and i_g are the input voltage and current, respectively, V_g and I_g are their RMS values, and ω_g is the grid angular frequency. In single-phase systems, the DC voltage of the AC-DC converter exhibits a ripple at twice the grid frequency. In order to compensate for this power pulsation, the APD method

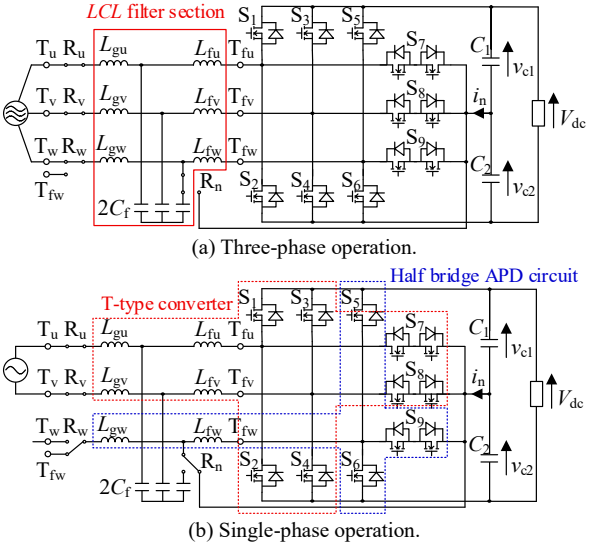


Fig. 1. Circuit configuration of the single-phase and three-phase compatible T-type converter.

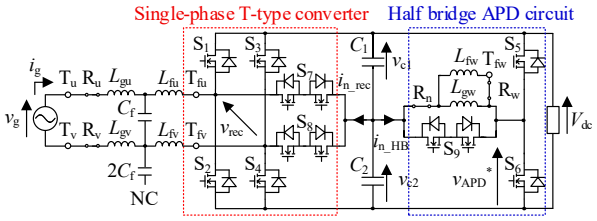


Fig. 2. Circuit diagram separating the T-type converter side and the APD circuit side in single-phase operation.

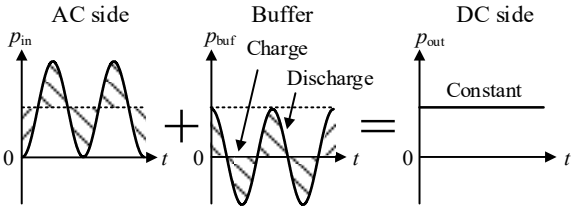


Fig. 3. Principle of active power decoupling method.

controls the buffer power p_{buf} in the opposite phase, as shown in Fig. 3.

In the T-type converter, the APD method regulates the DC-side capacitor voltages, v_{c1} and v_{c2}, as sinusoidal waveforms with opposite phases, centered around half the DC voltage. These voltages are expressed as

$$\begin{cases} v_{c1} = \dfrac{V_{dc}}{2} + V_c \sin(\omega_g t - \dfrac{\pi}{4}) \\ v_{c2} = \dfrac{V_{dc}}{2} - V_c \sin(\omega_g t - \dfrac{\pi}{4}) \end{cases} \quad V_c \le \frac{V_{dc}}{2} \tag{2}$$

where V_{dc} is the DC voltage, and V_c is the amplitude of the capacitor voltage, which must be less than half of V_{dc}. From (2), the neutral point current i_n, flowing through the leg formed by the DC-side capacitors is derived as

$$i_n = 2\omega_g C V_c \sin(\omega_g t + \frac{\pi}{4}) \tag{3}$$

where C is the capacitance of C_1 and C_2 ($C_1 = C_2$). By shaping the neutral point current i_n to match (3), the T-type converter achieves APD function without requiring any additional circuit.

III. Control Strategy

This section describes the control strategies for the T-type converter and the half-bridge APD circuit during single-phase operation.

A. T-type Converter

Fig. 4 shows the operating waveforms of the line voltage in the T-type converter with APD. Fig. 4(a) shows the waveform when operating between 0 V and the capacitor voltages v_{c1} and v_{c2}, while Fig. 4(b) shows the waveform when operating between V_{dc} and the capacitor voltages v_{c1} and v_{c2}. The T-type converter applies either v_{c1} or v_{c2} to the line voltage v_{rec} when the full-bridge-side switches (S_1 to S_4) and the neutral point switches (S_7, S_8) are turned on simultaneously. Since v_{c1} and v_{c2} differ from V_{dc}, the resulting line voltage v_{rec} forms a multi-level waveform. When v_{c1} and v_{c2} fluctuate for APD, a temporary imbalance in the voltage applied to v_{rec} occurs during each switching period. However, the duration for which each capacitor voltage is applied within a switching cycle remains constant. Moreover, since the capacitor voltages are sinusoidal waveforms with equal amplitude and opposite phase, no steady-state voltage error occurs even if the capacitor voltages fluctuate. No steady-state voltage error occurs in the negative half-cycle either, according to the same logic. Therefore, conventional carrier level-shift modulation can be applied to T-type converters with APD.

B. Half-bridge Active Power Decoupling Circuit

The current from each DC-side capacitor splits into two parts: i_{n_rec}, which flows into the T-type converter side, and i_{n_HB}, which flows into the half-bridge APD circuit as shown in Fig. 2. In this case, i_{n_rec} is sufficiently smaller than the current command i_{n_HB} as shown in (3). Thus, the i_{n_HB} compensates for both the capacitor voltage fluctuations caused by i_{n_rec} and the power pulsation component at twice the grid frequency.

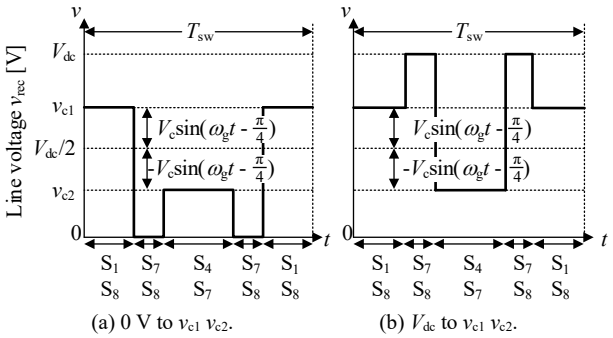
C. Control Block Diagram

Fig. 5 shows the control block diagram in single-phase operation. T-type converter side consists of output voltage control and grid current control. The modulation method is the conventional carrier level-shift technique. The voltage balancing control in APD circuit side compensates for imbalances caused by i_{n_rec}. Switches S_5 and S_6 operate based on the APD circuit output voltage command v_{APD}^* from the PI controller. The inductors L_{wg} and L_{wf}, through which i_{n_HB} flows, correspond to the w-phase in three-phase operation. Since a current sensor is already installed for this phase, no additional sensor is required for the APD circuit.

IV. Proposed Design Method of Capacitor Voltage Utilization Factor

This section describes a volume minimization design method for capacitor voltage utilization factor α. Single-phase applications require larger filter volumes per phase compared to three-phase systems. Thus, the proposed design method calculates LCL filter parameters based on single-phase circuit specifications. The capacitor voltage utilization factor is defined as the ratio of the peak-to-peak capacitor voltage to the DC voltage. The capacitor voltage utilization factor is defined as

$$\alpha = \frac{2V_c}{V_{dc}} \tag{4}$$



(a) 0 V to v_{c1} v_{c2}. (b) V_{dc} to v_{c1} v_{c2}.

Fig. 4. Operating waveforms of line voltage v_{rec} in the T-type converter with APD

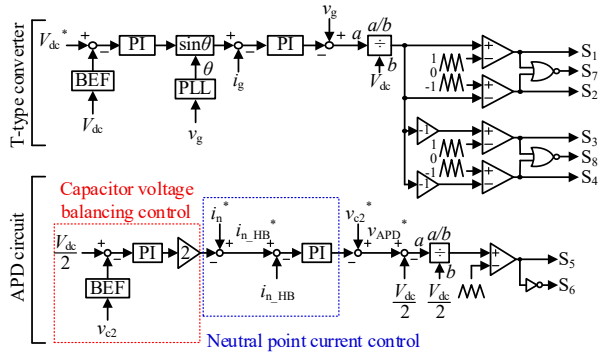


Fig. 5. Control block diagram in single-phase operation.

The capacitor voltage amplitude V_c must be less than or equal to $V_{dc}/2$, hence the capacitor voltage utilization factor α is defined as a value between 0 and 1.

A. Design of LCL Filters

The parameters of the *LCL* filter are designed based on the harmonic theoretical equation to satisfy the constraint conditions [13]. The constraint conditions for the *LCL* filter are shown as follows.

1. Grid current THD must be below the desired value δ_{THD}.
2. Reactive power ratio at or below the desired value λ_Q.
3. Resonance angular frequency ω_{res} of the *LCL* filter must be within the specified range.

The constraints include conditions for reactive power and resonance frequency, unlike Ref. [13]. As a result, compensation parameters based on experience are unnecessary. The constraint range for the resonance angular frequency ω_{res} is expressed as

$$10\omega_g \le \omega_{res} \le 0.5\omega_{fsw} \tag{5}$$

where ω_{fsw} is the switching angular frequency. This constraint is set to avoid resonance in both low-order and high-order harmonics [14].

The harmonic theoretical equation is required for *LCL* designs that satisfy the grid current THD constraint [13]. Harmonics in a typical single-phase T-type converter appear around even multiples of the switching frequency. On the other hand, when APD is applied, the harmonic component corresponding to the capacitor voltage utilization factor α is superimposed on the line voltage v_{rec}. The harmonic theoretical equation for line voltage v_{rec} considering capacitor voltage fluctuations is expressed as

$$
\begin{aligned}
v_{\mathrm{rec}} &= V_{\mathrm{dc}} M \cos \omega_{\mathrm{g}} t \\
&+ \frac{\sqrt{2}\alpha V_{\mathrm{dc}}}{\pi} \sum_{m=1}^{\infty} \frac{1}{2m-1} \sum_{n=-\infty}^{\infty} J_1\left\{(2m-1)\pi M\right\} \cos\left\{(2m-1)\omega_{\mathrm{g}} t\right\} \\
&+ \frac{\alpha V_{\mathrm{dc}}}{\pi} \sum_{m=1}^{\infty} \frac{1}{2m-1} \sum_{n=-\infty}^{\infty} \begin{bmatrix} A_{\mathrm{mn}} \cos\left\{(2m-1)\omega_{\mathrm{g}} t + 2n\omega_{\mathrm{fsw}} t\right\} \\ -B_{\mathrm{mn}} \sin\left\{(2m-1)\omega_{\mathrm{g}} t + 2n\omega_{\mathrm{fsw}} t\right\} \end{bmatrix} \\
&+ \frac{2V_{\mathrm{dc}}}{\pi} \sum_{m=1}^{\infty} \frac{1}{2m} \sum_{n=-\infty}^{\infty} J_{2n+1}\left\{2m\pi M\right\} \cos\left\{2m\omega_{\mathrm{g}} t + (2n+1)\omega_{\mathrm{fsw}} t\right\}
\end{aligned}
\tag{6}
$$

where

$$
\begin{aligned}
A_{\mathrm{mn}} &= (-1)^n \left\{J_{2n+1}\left\{m\pi M\right\} - J_{2n-1}\left\{m\pi M\right\}\right\} \\
B_{\mathrm{mn}} &= (-1)^n \left\{J_{2n+1}\left\{m\pi M\right\} + J_{2n-1}\left\{m\pi M\right\}\right\}
\end{aligned}
\tag{7}
$$

and where M is the modulation index, J_{n} is the Bessel function of the first kind. The validity of (6) and (7) has been verified [15]. Thus, the derivation process is omitted. The harmonic theoretical equation (6) indicates that harmonic components superimposed on the line voltage v_{rec} also increase as the capacitor voltage utilization factor α increases.

Fig. 6 shows the circuit model of the *LCL* filter. The *LCL* filter parameters are designed based on the single-phase model in Fig. 6(a). Fig. 6(b) shows the switching frequency model of the *LCL* filter. At the switching frequency, the impedance of the grid-tied inductor L_{g} is sufficiently larger than that of the filter capacitor C_{f}. As a result, the switching ripple current does not flow to the AC grid. Thus, the AC grid is effectively a short circuit.

In order to determine the parameters of the *LCL* filter, the switching frequency model shown in Fig. 6(b) is used. From Fig. 6(b), the switching frequency component current flowing through the converter $I_{\mathrm{conv\_fsw}}$ is expressed as

$$
| I_{\mathrm{conv\_fsw}} | = (\omega_{\mathrm{fsw}}{}^2 L_{\mathrm{g}} C_{\mathrm{f}} - 1) | I_{\mathrm{g\_fsw}} | = \beta | I_{\mathrm{g\_fsw}} |
\tag{8}
$$

where β is the current division ratio to $I_{\mathrm{conv\_fsw}}$. In order to simplify the calculations, the inductance ratio γ is defined. Using the inductance ratio γ, the grid-tied inductance L_{g} is expressed as

$$
L_{\mathrm{g}} = \gamma L_{\mathrm{f}}
\tag{9}
$$

Using (8)-(9), the harmonic component of the grid current $I_{\mathrm{g\_fsw}}$ is expressed as

$$
I_{\mathrm{g\_fsw}} = \frac{V_{\mathrm{conv\_fsw}}}{\omega_{\mathrm{fsw}} L_{\mathrm{f}} (\beta - \gamma)}
\tag{10}
$$

where $V_{\mathrm{conv\_fsw}}$ is the harmonic voltage of the T-type converter with APD. In other words, $V_{\mathrm{conv\_fsw}}$ represents a spectrum other than the fundamental spectrum in (6). From the grid current THD constraint δ_{THD} and (10), the filter inductor L_{f} is expressed as

$$
L_{\mathrm{f}} \geq \frac{V_{\mathrm{conv\_fsw}}}{\omega_{\mathrm{fsw}} \delta_{\mathrm{THD}} I_{\mathrm{g}} (\beta - \gamma)} = \frac{L_0}{\beta - \gamma}
\tag{11}
$$

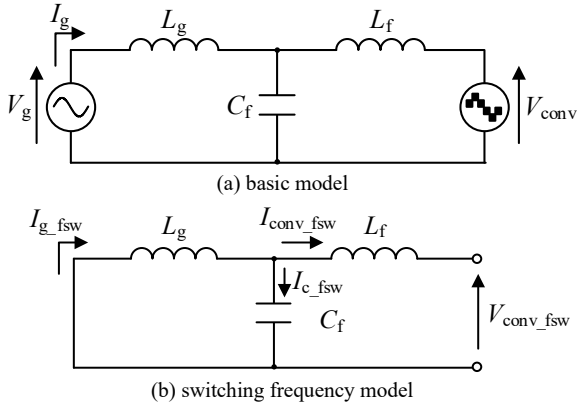


Fig. 6. Circuit model of the LCL filter.

where L_0 is the normalized inductance that is independent of the current divided ratio β and the inductance ratio γ. The normalized inductance L_0 is expressed as

$$
L_0 = \frac{V_{\mathrm{conv\_fsw}}}{\omega_{\mathrm{fsw}} \delta_{\mathrm{THD}} I_{\mathrm{g}}}
\tag{12}
$$

The *LCL* parameters represented by normalized inductance L_0 (12) are expressed as

$$
L_{\mathrm{f}} = \frac{L_0}{\beta - \gamma},\ L_{\mathrm{g}} = \frac{\gamma L_0}{\beta - \gamma},\ C_{\mathrm{f}} = \frac{\beta + 1}{\omega_{\mathrm{fsw}}{}^2 L_0} \frac{\beta - \gamma}{\gamma}
\tag{13}
$$

The filter capacitance is limited by the reactive power ratio constraint λ_{Q}. This constraint λ_{Q} is defined as a ratio relative to the rated power. Thus, the upper limit of the filter capacitance C_{f} is expressed as

$$
C_{\mathrm{f}} \leq \frac{\lambda_{\mathrm{Q}} P_{\mathrm{out}}}{\omega_{\mathrm{g}} V_{\mathrm{g}}{}^2}
\tag{14}
$$

The parameters of the *LCL* filter are determined using (12)-(14). Thus, the resonance angular frequency ω_{res} is expressed by the current divided ratio β and the inductance ratio γ. As a result, the resonance angular frequency ω_{res} is expressed as

$$
\omega_{\mathrm{res}} = \sqrt{\frac{1+\gamma}{1+\beta}} \omega_{\mathrm{fsw}}
\tag{15}
$$

Furthermore, the analysis range for the current divided ratio β is obtained using (5) and (15) as

$$
4\gamma + 3 \leq \beta \leq (1+\gamma) \left(\frac{\omega_{\mathrm{fsw}}}{10\omega_{\mathrm{g}}} \right)^2 - 1
\tag{16}
$$

The analysis range for the inductance ratio γ is set to any range around one. By using (6)-(7), (12)-(14), and (16), the parameters of the *LCL* filter are determined. After calculating each parameter, the volume of the *LCL* filter is calculated. The volume of the capacitor is calculated based on the capacitance and the energy density per unit volume. The filter capacitor is designed based on the specifications of the MKP Series from

TDK. The volume of the inductor is calculated based on the area product method. The volume of the inductor is expressed as

$$Vol_{\mathrm{L}} = K_{\mathrm{v}} \left(\frac{L I_{\max}{}^{2}}{K_{\mathrm{u}} B_{\mathrm{s}} J} \right)^{\frac{3}{4}} \tag{17}$$

B. Design of DC-side Capacitors

From (1)-(4), the capacitance of the DC-side capacitor is expressed as

$$C_1 = C_2 = \frac{4P_{\mathrm{out}}}{\omega_{\mathrm{g}} (\alpha V_{\mathrm{dc}})^2} \tag{18}$$

The volume of the DC-side capacitor is calculated based on the energy density per unit volume, the same as for the filter capacitor C_{f}. Energy density is calculated based on the WIMA DCP series film capacitors.

C. Design of Heat sink

The worst-case losses caused by switching devices must be calculated in order to determine the heat sink volume. Thus, the losses in the half-bridge side and neutral-point side of both the T-type converter and the APD circuit are calculated. Since applying APD has no effect on the conduction losses in the T-type converter side, the conduction losses are calculated using the existing theoretical equation [16]. Assuming a unity power factor, the conduction losses caused by the T-type converter side are expressed as

$$\begin{cases} P_{\mathrm{cond\_s1}} = P_{\mathrm{cond\_s2}} = P_{\mathrm{cond\_s3}} = P_{\mathrm{cond\_s4}} = \dfrac{2\sqrt{2}M}{3\pi} R_{\mathrm{on}} I_{\mathrm{g}} \\ P_{\mathrm{cond\_s7}} = P_{\mathrm{cond\_s8}} = R_{\mathrm{on}} I_{\mathrm{g}}{}^{2} \end{cases} \tag{19}$$

where R_{on} is the on-resistance of the switching device. Please note that $P_{\mathrm{cond\_s7}}$ and $P_{\mathrm{cond\_s8}}$ each represent the losses of two switching devices. When APD is applied, the voltage applied to the switching devices on the T-type converter side changes. Therefore, the capacitor voltage fluctuation is considered in the theoretical equation in Ref. [16]. Assuming that the capacitor voltages are matched to (2), the switching losses on the T-type converter side are expressed as

$$\begin{cases} P_{\mathrm{sw\_s1}} = P_{\mathrm{sw\_s2}} = P_{\mathrm{sw\_s3}} = P_{\mathrm{sw\_s4}} \\ \qquad = \dfrac{\sqrt{2} f_{\mathrm{sw}} (e_{\mathrm{on}} + e_{\mathrm{off}}) V_{\mathrm{dc}} I_{\mathrm{g}}}{2\pi E_{\mathrm{dcd}} I_{\mathrm{md}}} \left(1 + \dfrac{\alpha\pi}{4\sqrt{2} V_{\mathrm{dc}}} \right) \\ P_{\mathrm{sw\_s7}} = P_{\mathrm{sw\_s8}} = \dfrac{\sqrt{2} f_{\mathrm{sw}} (e_{\mathrm{on}} + e_{\mathrm{off}}) V_{\mathrm{dc}} I_{\mathrm{g}}}{\pi E_{\mathrm{dcd}} I_{\mathrm{md}}} \left(1 + \dfrac{\alpha\pi}{4\sqrt{2} V_{\mathrm{dc}}} \right) \end{cases} \tag{20}$$

where f_{sw} is the switching frequency, e_{on} is the turn-on loss, e_{off} is the turn-off loss, E_{dcd} is the measurement voltage for the turn-on and turn-off losses specified in the datasheet and I_{md} is the current during losses measurement. Note that the APD circuit controls the neutral-point current rather than the grid current, then derive theoretical equations for conduction losses and switching losses based on the neutral point current i_{n}. The conduction losses and switching losses on the APD circuit side are expressed as

$$P_{\mathrm{cond\_s5}} = P_{\mathrm{cond\_s6}} = \frac{R_{\mathrm{on}} I_{\mathrm{n}}{}^{2}}{2} \tag{21}$$

$$P_{\mathrm{sw\_s5}} = P_{\mathrm{sw\_s6}} = \frac{2\sqrt{2} f_{\mathrm{sw}} V_{\mathrm{dc}} I_{\mathrm{n}} (e_{\mathrm{on}} + e_{\mathrm{off}})}{\pi E_{\mathrm{dcd}} I_{\mathrm{md}}} \tag{22}$$

where I_{n} is the RMS value of the neutral point current i_{n}. Calculate the losses in (19)-(22) under rated power conditions and identify the switching device with the worst loss. The identification of the worst-case loss is not limited to single-phase operation. If the loss when operating as a three-phase T-type is the worst-case loss, that value is used. In the case of operation as a three-phase T-type converter, use the three-phase circuit specifications and set $\alpha = 0$ in (20). Calculate the thermal resistance of the heat sink $R_{\mathrm{th(h-a)}}$ so that the junction temperature of the switching device remains below the desired junction temperature $T_{\mathrm{j\_limit}}$. The thermal resistance of the heat sink $R_{\mathrm{th(h-a)}}$ is expressed as

$$R_{\mathrm{th(h-a)}} = \frac{T_{\mathrm{j}} - T_{\mathrm{a}} - P_{\mathrm{loss}} R_{\mathrm{th(j-c)}} - P_{\mathrm{total}} R_{\mathrm{th(c-h)}}}{P_{\mathrm{total}}} \tag{23}$$

where T_{a} is the ambient temperature, P_{loss} is worst-case loss in all switching devices, P_{total} is the total loss of the switching device, $R_{\mathrm{th(j-c)}}$ is the thermal resistance from the junction to the case in the switching device with the worst-case loss, and $R_{\mathrm{th(c-h)}}$ is the thermal resistance from the case to the heat sink. The heat sink design is based on Cooling System Performance Index (CSPI) [17]. From the thermal resistance of the heat sink and the CSPI, the heat sink volume is expressed as

$$Vol_{\mathrm{HS}} = \frac{1}{R_{\mathrm{th(h-a)}} CSPI} \tag{24}$$

D. Calculation of Capacitor Voltage Utilization Factor

Fig. 7 shows the flowchart for calculating the capacitor voltage utilization factor α. The capacitor voltage utilization factor α is calculated to satisfy the constraints while minimizing the total volume. As the first step, the volume of the *LCL* filter is calculated when the current divided ratio β and inductance ratio γ are changed. Among the *LCL* filters that satisfy the constraints, the one with the smallest volume is selected for each capacitor voltage utilization factor α. Next, the volume of the DC-side capacitor is calculated based on the capacitor voltage utilization factor α. Then, the heat sink volume is calculated based on the worst-case losses of the switching devices during single-phase operation or three-phase operation. Finally, the calculated value of the capacitor voltage utilization factor α that results in the minimum total volume is selected.

TABLE I. INPUT PARAMETERS

Parameter	Symbol	Value
Output power	$P_{out\_single\text{-}phase}$	3 kW
	$P_{out\_three\text{-}phase}$	11 kW
DC voltage	V_{dc}	450 V
Grid voltage	$V_{g\_single\text{-}phase}$	200 V
	$V_{g\_three\text{-}phase}$	380 V
Grid frequency	f_g	50 Hz
Switching frequency	f_{sw}	20 kHz
Volume coefficient	K_v	18.1
Window utilization factor	K_u	0.4
Saturated magnetic flux	B_s	200 mT
Current density	J	4.0 A/mm^2
Energy density (C_f)	-	23.2 kJ/m^3
Energy density (C_1,C_2)	-	220 kJ/m^3
Minimum inductance ratio	γ_{min}	0.5
Maximum inductance ratio	γ_{max}	2.0
THD constraint	δ_{THD}	3.0 %
Reactive power constraint	λ_Q	1.0 %
Current margin	-	1.1
Drain-Source resistance	R_{on}	8.3 mΩ
Turn-on switching loss	e_{on}	1.01 mJ
Turn-off switching loss	e_{off}	0.80 mJ
Junction temperature	T_j	100 °C
Ambient temperature	T_a	25 °C
Thermal resistance junction to case (Half bridge)	$R_{th(j\text{-}c)\_HB}$	0.635 K/W
Thermal resistance junction to case (T-type)	$R_{th(j\text{-}c)\_T\text{-}type}$	0.790 K/W
Thermal resistance case to heatsink	$R_{th(c\text{-}h)}$	1.0 K/W
Cooling system performance index	CSPI	10

Table 1 shows the input parameters. The maximum current of each inductor is set with a margin of 1.1 times the amplitude, considering switching ripple. In addition, the volume coefficient of the inductors is based on the values measured in the prototypes. The capacitor voltage utilization factor α is swept from 0 to 1 with a step of 0.001.

Fig. 8 shows the calculation results for the *LCL* filter. The horizontal axis represents the inductance ratio γ, and the vertical axis represents the current divided ratio β. The upper part of Fig. 8 represents the region that does not satisfy the reactive power constraint. This is due to the fact that a large value of β resulted in the calculation of a filter capacitor C_f that does not satisfy the reactive power constraint. In contrast, the lower part of Fig. 8 represents the region that does not satisfy the analysis range (16).

Fig. 9 shows the calculation results for each volume when the capacitor voltage utilization factor is changed. Table 2 shows the parameters at the volume minimization point. Under the conditions as shown in Table 1, the volume minimization value for the capacitor voltage utilization factor α is 0.773. In the calculated *LCL* filter, both the grid-tied inductor L_g and the filter inductor L_f are 160 μH. The filter capacitor C_f is 2.4 μF. The resonant angular frequency ω_{res} calculated from the calculated *LCL* parameters is $51.2*10^3$ rad/s, which satisfies (5).

V. EXPERIMENTAL RESULTS

Table 3 shows the experimental conditions. Since the capacitance of the DC-side capacitor is adjusted by the number of capacitors in parallel, it is not possible to set it exactly equal to the calculated value. For this reason, the capacitance is set to 300 μF compared to the calculated value of 316 μF.

A. Fundamental Operation

Fig. 10 shows the experimental results of the T-type converter in single-phase grid operation. Fig. 10(a) shows the result without APD, while Fig. 10(b) shows the result with APD. The capacitor voltages v_{c1} v_{c2}, and output voltage V_{dc} pulsate at twice the grid frequency due to power pulsations as demonstrated in Fig. 10(a). Consequently, the pulsation component is superimposed on the line voltage v_{rec}. In contrast,

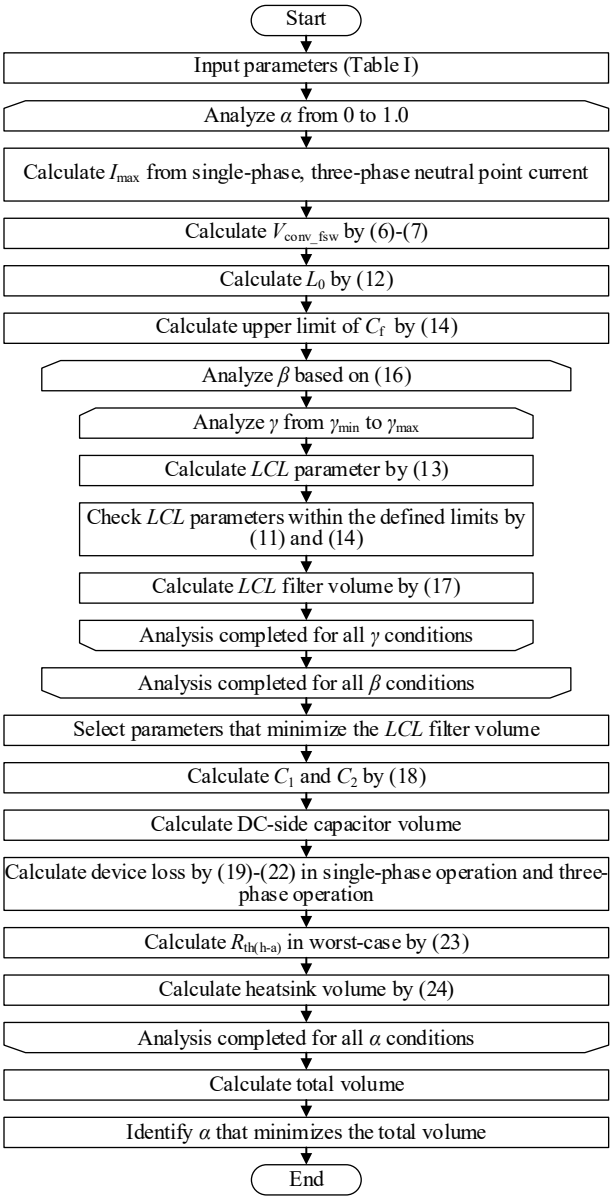


Fig. 7. Flowchart for calculating the capacitor voltage utilization factor.

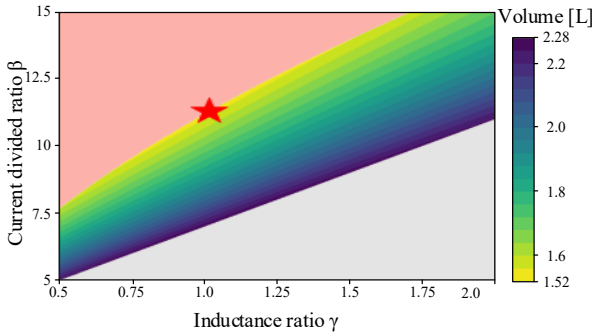


Fig. 8. Calculation results for the *LCL* filter.

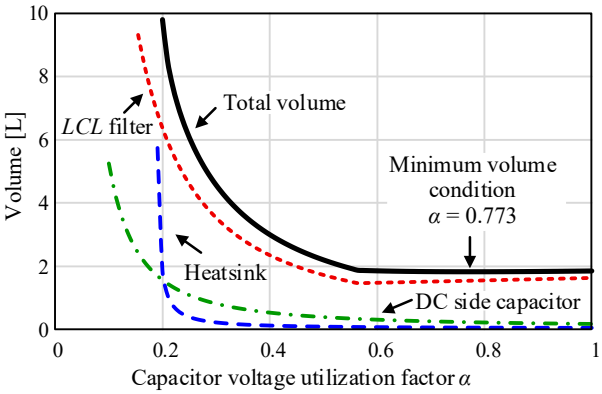


Fig. 9. Calculation results for each volume when the capacitor voltage utilization factor is changed.

the output voltage V_{dc} remains constant in Fig. 10(b). This indicates that the DC-side capacitors C_1 and C_2 operate as energy buffers due to the applied APD. The evidence for this is the neutral point current i_n flowing in Fig. 10(b). However, the grid current ripple increases as shown in Fig. 10(b). This is caused by the significant pulsation of the capacitor voltages v_{c1} and v_{c2} due to the APD capability.

Fig. 11 shows the efficiency and THD characteristics of the proposed system. The maximum efficiency without APD is 99.2% at 1.5 kW, and with APD is 96.8% at 2.5 kW. The APD circuit decreases efficiency by allowing neutral point current i_n to flow that is larger than the grid current i_g. Additionally, the APD circuit employs two-level modulation, in contrast to the T-type converter. This also leads to decreased efficiency. The grid current THD is calculated up to the 40th harmonic of the fundamental frequency. The grid current THD at rated power is 0.5% without APD and 0.9% with APD. Although APD operation increases the harmonic components of the line voltage v_{rec} due to the capacitor voltage fluctuation described in (6), the grid current THD still satisfies the constraint δ_{THD} as shown in Table 2, owing to the *LCL* filter design.

B. Harmonic Analysis of DC Voltage

Fig. 12 shows the harmonic analysis of the DC voltage V_{dc}. The fundamental frequency is 50 Hz, and each harmonic component is normalized to the DC component. The second-order harmonic component with the APD function is reduced to 0.2%, representing a 99.5% reduction compared to the case without APD. However, a small second-order harmonic component remains in the DC voltage V_{dc}. The reason for this is the error introduced by neglecting the reactive power of the w-phase inductors when deriving the capacitor voltages v_{c1}, v_{c2}, and neutral point current i_n. Nevertheless, the results in Fig. 12 demonstrate sufficient effectiveness in reducing the second-order harmonic, confirming the validity of the proposed APD method.

TABLE II. PARAMETERS AT THE VOLUME MINIMIZATION POINT

Parameter	Symbol	Optimal value
Capacitor voltage utilization factor	α	0.773
DC-side capacitor	C_1, C_2	316 μF
Grid-tied inductor	L_{gu}, L_{gv}, L_{gw}	160 μH (%Z:0.38%)
Filter inductor	L_{fu}, L_{fv}, L_{fw}	160 μH (%Z:0.38%)
Filter capacitor	C_{fu}, C_{fv}, C_{fw}	2.4 μF
Resonant angular frequency	ω_{res}	$51.2*10^3$ rad/s

TABLE III. EXPERIMENTAL CONDITIONS

Parameter	Symbol	Value
Output power	P_{out}	3 kW
Grid voltage	v_{in}	200 V_{rms}
Output voltage	V_{dc}	450 V
Grid frequency	f_g	50 Hz
Switching frequency	f_{sw}	20 kHz
DC-side capacitor	C_1, C_2	300 μF
Capacitor voltage utilization factor	α	0.793
Grid-tied inductor	L_{gu}, L_{gv}, L_{gw}	170 μH (%Z:0.4%)
Filter inductor	L_{fu}, L_{fv}, L_{fw}	170 μH (%Z:0.4%)
Filter capacitor	C_{fu}, C_{fv}, C_{fw}	2.0 μF
Switching device	S_1~S_9	F3L8MXTR12C2M2_H11

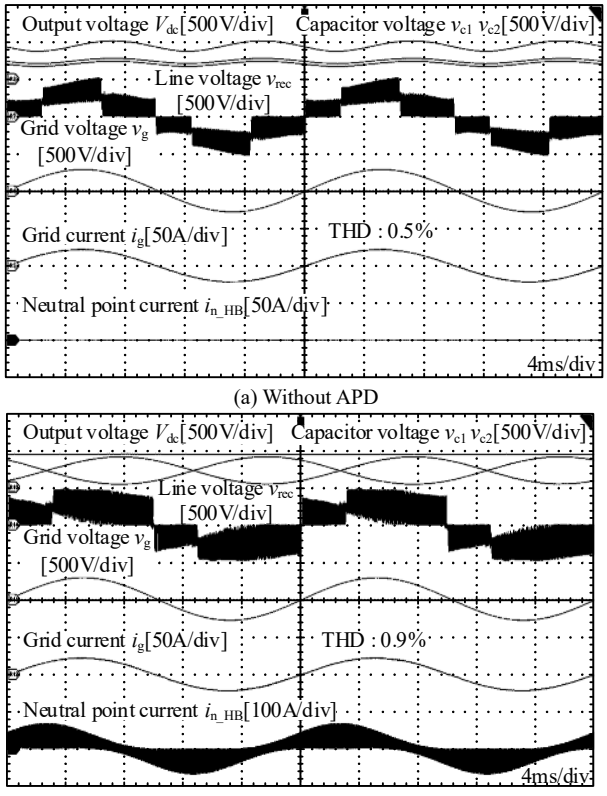


Fig. 10. Experimental results in steady state.

VI. CONCLUSION

This paper proposed a volume minimization design method for the capacitor voltage utilization factor α to minimize the total system volume in a single-phase and three-phase compatible T-type converter with APD capability. The proposed method determines the capacitor voltage utilization factor α that minimizes the total system volume while

satisfying constraints on grid current THD and reactive power ratio by analyzing the quantitative trade-offs between the volumes of the *LCL* filter designed via a harmonic theoretical equation, the DC-side capacitors, and the heat sink considering switching losses. Experimental results showed that the second-order harmonic component of the DC voltage is reduced by 99.5% compared to the case without APD. At this minimization design point, the system achieved a maximum efficiency of 96.8% at 2.5 kW, while the grid current THD at rated power was 0.9%. These results validated the effectiveness of the proposed volume minimization method.

ACKNOWLEDGMENT

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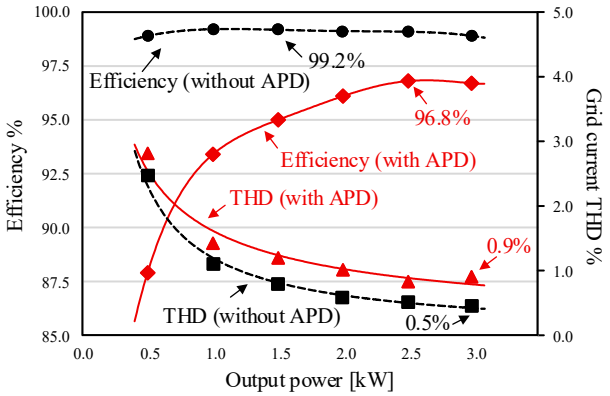

Fig. 11. Characteristics of efficiency and grid current THD.

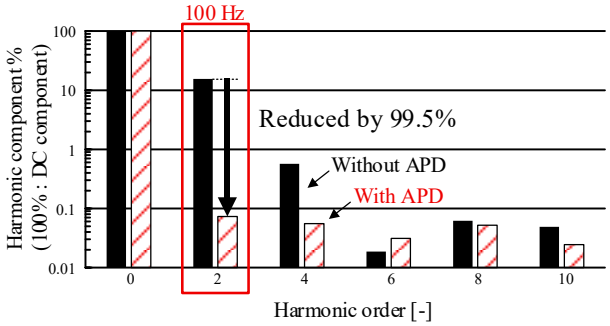

Fig. 12. Harmonic analysis result of the DC voltage.

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