Experimental Verification of Current Balancing in Parallel MHz WPT Systems Using a Coupled Inductor Pair

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***Abstract*— This paper proposes a current balancer using a coupled-inductor pair with leakage-inductance compensation for MHz wireless power transfer (WPT) systems. A conventional balancer consisting of coupled inductors and series capacitors suppresses short-circuit currents caused by inverter common mode voltage differences and circulating currents caused by voltage imbalance. However, in MHz applications, low-permeability magnetic materials reduce the coupling coefficient, increasing leakage inductance and reducing transmitted power. The proposed configuration compensates for the leakage inductance using parallel capacitors, achieving power transfer while maintaining current balance. The current-balancing performance is verified using a 1-kW-class prototype with a resonant load. Experimental results show imbalance ratios of 9.16% and 9.72% at phase differences of 0° and 20°, respectively. Therefore, the proposed balancer suppresses the increase in the circulating current even under voltage imbalance.**

Keywords*— *Wireless Power Transfer, Megahertz inverter, current balancer, coupled inductor, circulating current

I. INTRODUCTION

Wireless power transfer (WPT) has been widely studied as a contactless power supply technology for electric vehicles (EVs) and industrial equipment [1][2]. These applications require high power, while recent applications to mobile platforms such as drones and automated guided vehicles (AGVs) demand both compactness and high power density. High-frequency operation is an effective approach to increasing power density, and WPT in the megahertz range has been reported to achieve both high efficiency and high power density [3][4]. In megahertz-range WPT systems, gallium nitride (GaN) devices are widely used as the primary-side high-frequency voltage source due to their fast switching and low-loss characteristics [5][6]. However, their small chip area results in low thermal capacitance, which limits heat dissipation capability. Consequently, the output power of a single high-frequency inverter is typically limited to several kilowatts [5–7].

To increase the output power, multiple inverters are connected in parallel [7]. However, mismatches in switching devices, gate drivers, and wiring impedances cause voltage imbalance, which generates circulating current among the inverters. This circulating current reduces efficiency and increases device stress, making current balancing essential [9]. Current balancing methods can be classified into active and passive approaches. Active methods control the duty ratio or phase shift to achieve current sharing [7], but their performance degrades in the megahertz range due to nanosecond-level timing constraints and implementation mismatches. Passive methods achieve current balancing through circuit design, such as resonant current sharing [8] and coupled-inductor-based approaches [9]. These methods are suitable for high-frequency operation because they do not require additional control. However, these passive methods exhibit limitations in megahertz-range WPT systems. The resonant current-sharing method in [8] relies on the resonant condition and is therefore sensitive to variations in coupling coefficient and load, leading to degradation of both current sharing and power transfer. The coupled-inductor method in [9] effectively suppresses circulating current by adding impedance only to the unbalanced component. However, to achieve low loss at high frequency, low-permeability magnetic material must be used, which reduces the coupling coefficient and increases leakage inductance. This leakage inductance disturbs the resonant condition, resulting in reduced transferred power even when current balance is maintained.

The authors previously proposed a coupled-inductor-based current balancer [10], which selectively suppresses unbalanced and common-mode currents while minimally affecting the balanced component. Although effective for current balancing, its application to megahertz-range WPT reveals that leakage inductance significantly degrades power transfer. Therefore, achieving both current balance and power transfer remains a challenge.

This paper proposes a parallel capacitor across the coupled inductor to compensate for its leakage inductance and improve the inverter-side power factor. A parallel capacitor is introduced across the coupled inductor to form a resonant network that improves the power factor seen from the inverter. As a result, both current balance and efficient power transfer can be achieved even under low coupling conditions. The main contribution of this paper is to propose a leakage-inductance-compensation structure analogous to LCC compensation, which improves the inverter-side power factor and enables both current balancing and efficient power transfer in megahertz-range WPT systems. The operating principle of the proposed balancer is clarified based on balanced, unbalanced, and common-mode components. Its effectiveness is verified through experiments using a 6.78-MHz, 1-kW-class prototype, which demonstrates that the proposed method significantly improves power transfer while maintaining current balance.

II. Proposed System

A. Conventional System

Fig. 1 shows the configuration of a current balancer using a coupled inductor with a high coupling coefficient. The configuration consists of two split resonant capacitors and a pair of coupled inductors. Each winding of the coupled inductor is connected to the inverter arms that generate the same output voltage. The resonant capacitor is divided into two parts, each connected in series with a winding of the coupled inductor. Thus, the coupled inductor generates an induced voltage only when the inverter output voltages differ. In other words, the coupled inductor introduces impedance only to the imbalance component of the inverter output voltages, whereas no induced voltage is generated for the balanced component. As a result, the circulating current caused by the imbalance component of the inverter voltages is suppressed. In addition, the coupled inductor and the two split resonant capacitors also introduce impedance to the difference in the reference potentials of the inverters, thereby suppressing the short-circuit current caused by differences in the supply potentials. However, a large impedance is required to sufficiently suppress the circulating current and the short-circuit current. Therefore, magnetic materials are typically used in the coupled inductor. In the MHz frequency range, however, magnetic materials with high permeability are difficult to use because they cause significant core loss. For this reason, magnetic materials with relatively low permeability, such as NiZn ferrite or powder cores, are commonly used. However, the low permeability reduces the coupling coefficient. As the coupling coefficient decreases, the leakage inductance becomes non-negligible, resulting in a reduction in the power factor.

B. Circuit operation

Figs. 2(a)–(c) illustrate the operation of the proposed system for the balanced, unbalanced, and common-mode components of the inverter output voltage. The output voltage of each inverter is decomposed into these three components. The balanced component has identical amplitude and phase for all inverters. The unbalanced component represents the voltage difference between the inverters. The common-mode component corresponds to the voltage that varies in phase at the inverter terminals with respect to ground.

The balanced component contributes to power transfer. When only this component is considered, the currents flowing through all windings of the coupled-inductor pair are equal. If the coupling coefficient of the coupled inductors is close to unity, the voltages induced by self-inductance and mutual inductance cancel each other. As a result, the coupled inductors present almost no impedance to the balanced component, and the proposed balancer does not interfere with power transfer.

In contrast, the unbalanced component corresponds to the voltage difference between the inverter outputs and appears as voltage sources with opposite polarity for the two inverters. The current produced by the unbalanced component does not flow through the transmission coil but circulates between the inverters. Consequently, the voltages induced by self-inductance and mutual inductance in each winding appear in phase. As a result, the proposed balancer presents high impedance to the unbalanced component and suppresses the circulating current between the inverters. In addition, the series capacitors do not resonate with the transmission coil for this component and therefore also present impedance, which further contributes to the suppression of the circulating current.

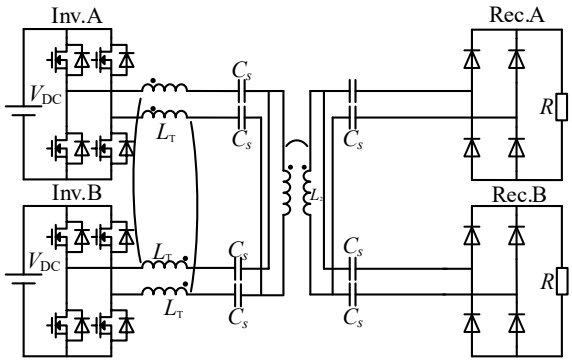
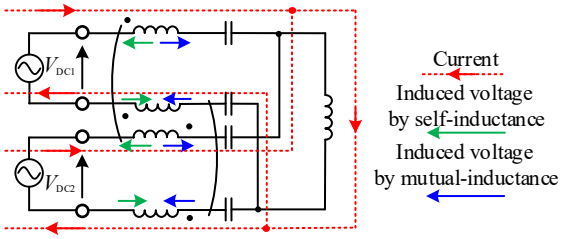
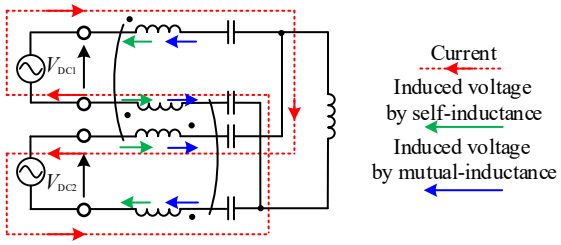


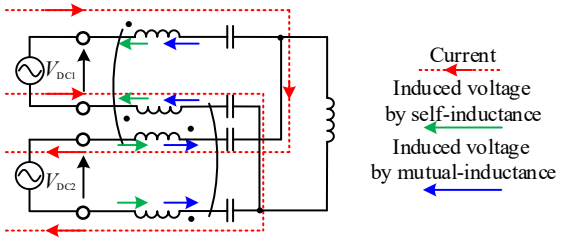
Fig. 1. WPT system with strongly coupled inductors.



(a) Induced voltages and current paths of balanced components



(b) Induced voltages and current paths of unbalanced components



(c) Induced voltages and current paths of common-mode operation

Fig. 2. Operation of each component in current balancer.

The common-mode component corresponds to the voltage that varies in phase at the inverter output terminals with respect to ground. Even when the common-mode voltages of the inverters differ, the resulting current does not flow through the transmission coil but flows only between the inverters. In this case, the proposed balancer presents a series impedance consisting of the coupled inductors and the series capacitors, providing sufficiently high impedance to the common-mode current.

The proposed balancer therefore presents almost no impedance to the balanced component that contributes to power transfer, while presenting high impedance to the unbalanced and common-mode components. As a result, circulating and common-mode currents generated during

parallel inverter operation are effectively suppressed without degrading power transfer.

C. Proposed system

Fig. 3 shows the circuit configuration of the proposed system, which compensates for leakage inductance. This configuration is similar to the LCC compensation topology commonly used in WPT systems. Therefore, the capacitances of the proposed system can be designed in the same manner as those of the LCC compensation topology. The resonance condition of the LCC compensation is given by

$$\omega = \frac{1}{\sqrt{2(1-k_{Tn})L_{Tn}C_{pn}}} = \frac{1}{\sqrt{L_n \dfrac{C_{sn}C_{pn}}{C_{sn}+2C_{pn}}}} \qquad (n=1,\ 2) \tag{1}$$

The coupling coefficient of the coupled inductor is k_T. The self-inductance of the coupled inductor is L_T, the parallel capacitor is C_p, and the series capacitor is C_s. However, to reduce the conversion loss of the inverter, zero-voltage switching (ZVS) must be achieved. Therefore, the filter capacitance should be designed larger than the value calculated from (1) so that the input impedance seen by the inverter becomes inductive.

The transmitted power determines the inductance of the transmission coil, and the impedance for the circulating current determines the self-inductance of the coupled inductor. As a result, the parallel capacitor enables power transmission without being affected by the leakage inductance even when the coupling coefficient of the coupled inductor is low.

III. Simulation of the Proposed System

Fig. 4 shows the simulation and experimental configurations and parameters used to verify the effectiveness of the proposed balancer. In the WPT system, the proposed balancer is inserted on both the primary and secondary sides; their operations are independent. Therefore, in this verification, a load resistor is connected in series with the transmission coil, and only the primary-side operation is evaluated. The DC voltage is 135 V, and the switching frequency is 6.78 MHz. The self-inductance and coupling coefficient of the coupled inductor are 13.8 μH and 0.934, respectively. The load resistance is 25 Ω, and a 2.1-μH air-core inductor is used to emulate the transmission coil. Under this condition, the load Q-factor is 3.5. The parallel and series capacitances are 580 pF and 747 pF, respectively. These values are determined from the measured values of the fabricated coupled inductor and resonant inductor, considering (1) and the achievement of ZVS. In this paper, the cases with phase differences in the inverter output voltage of 0 ns and 8.19 ns (20 deg.) are compared for verification. The 8.19-ns condition corresponds to the assumed worst-case total delay caused by variations in the wiring impedance, devices, and drivers.

Fig. 5 shows the simulation results for the configuration without the parallel capacitor using a coupled inductor with a coupling coefficient of 0.943. The phase difference in the output voltage between the inverters is 20 deg. The currents of primary-side inverters A and B are 0.61 A and 0.60 A, respectively. These results confirm that the proposed balancer effectively equalizes the inverter output currents. In contrast,

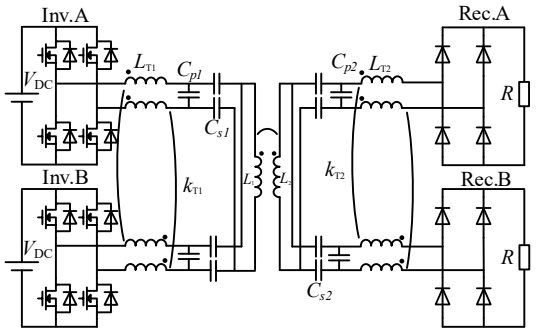


Fig. 3. Proposed WPT system with weakly coupled inductors.

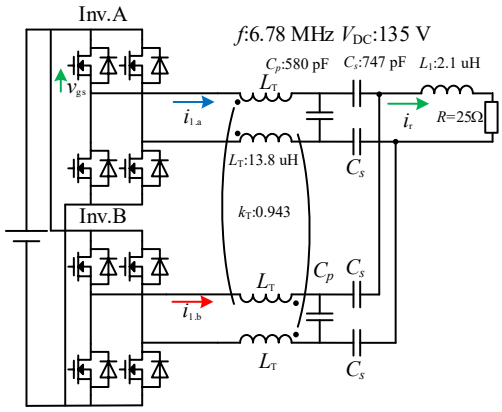


Fig.4. Experimental configuration to verify current balancing by the proposed balance with a resonance load.

the transmitted power is 36.9 W. This is because the leakage inductance of the coupled inductor increases to 1.18 μH, shifting the resonant frequency to 3.42 MHz and thereby preventing efficient power transfer. Therefore, although the conventional configuration can achieve current balancing by means of the coupled inductor, its power-transfer performance deteriorates because of the leakage inductance.

Fig. 6 shows the simulation results for the proposed circuit with the added parallel capacitor. In the proposed configuration, the inverter output currents $i_{inv.a}$ and $i_{inv.b}$ are 7.82 A and 7.81 A, respectively. Therefore, the results confirm that the proposed balancer equalizes the currents. In addition, the transmitted power reaches 1.22 kW in the proposed circuit, indicating a significant improvement in power transfer compared with the conventional configuration. These results demonstrate that the proposed method maintains current balance while enabling power transfer even when a coupled inductor with a low coupling coefficient is used.

IV. Experimental Verification

A. Operation waveform

Figs. 7(a) and 7(b) show the inverter output voltages $v_{inv.a}$ and $v_{inv.b}$ and the inverter output currents $i_{inv.a}$ and $i_{inv.b}$, respectively, whereas Figs. 7(c) and 7(d) show the harmonic analysis results of the circulating current. Here, the circulating current is defined as the difference between the output currents of the two inverters and is obtained using the arithmetic function of the oscilloscope. Figs. 7(a) and 7(c) show the operation when there is no phase difference between the

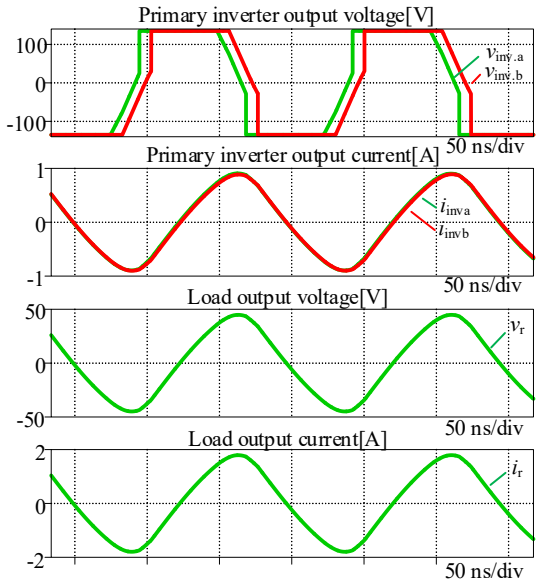


Fig.5. Simulation result of conventional system at coupling coefficient of 0.9.

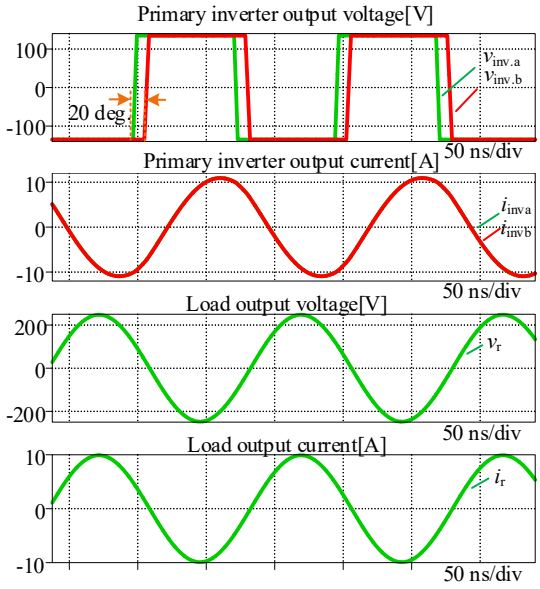
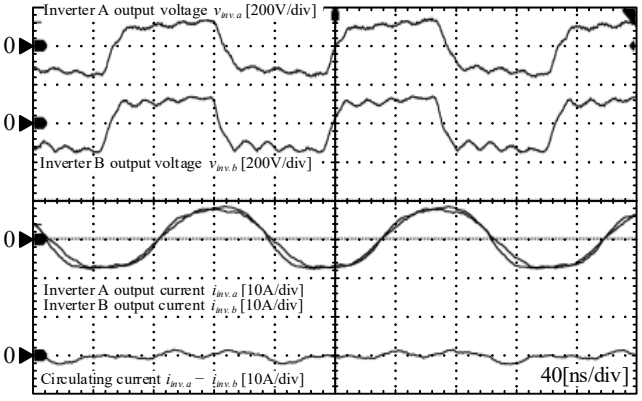
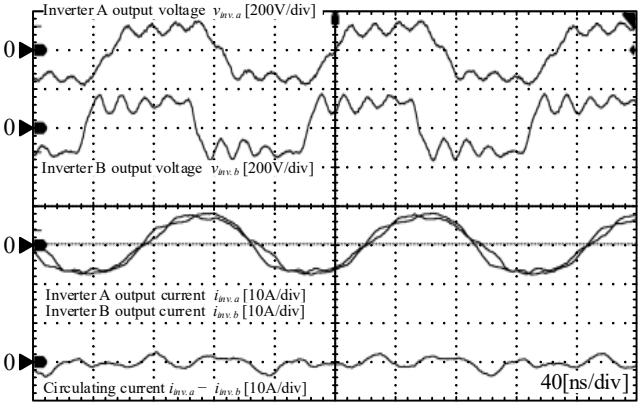


Fig.6. Simulation result of proposed system at coupling coefficient of 0.9.

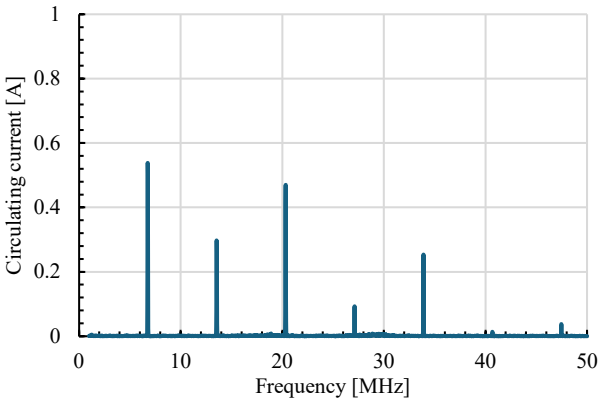
output voltages. In this case, the inverter output currents are $i_{inv.a}$ = 6.14 A and $i_{inv.b}$ = 5.61 A, and the fundamental component of the circulating current $i_{inv.a} - i_{inv.b}$ is 538 mA. By contrast, Figs. 7(b) and 7(d) show the case in which the phase difference between the output voltages of the inverters is 20 degrees. In this case, the inverter output currents are 5.74 A and 5.23 A for Inv. A and Inv. B, respectively, and the circulating-current component is 533 mA. Furthermore, the harmonic analysis results indicate that the circulating current contains significant third- and fifth-order harmonic components in addition to the fundamental component. This is because the impedance for the third- and fifth-order harmonics is reduced due to the interwinding capacitance of the coupled inductor. The imbalance factor is defined to evaluate the circulating current. The imbalance factor is defined as the ratio of the circulating current to the average value of the inverter currents and is expressed by



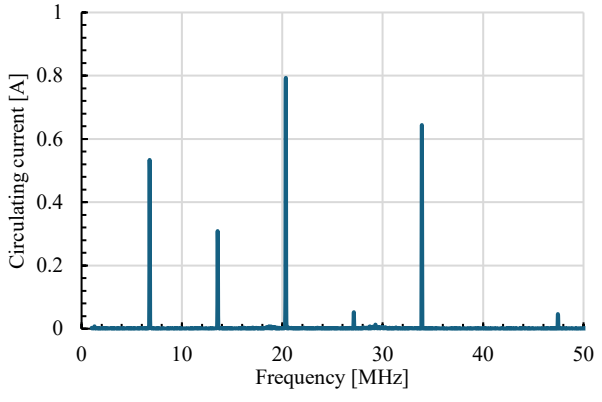
(a) without a phase difference of the proposed system.



(b) with a phase difference of 20°.



(c) without a phase difference of the proposed system.



(d) with a phase difference of 20°

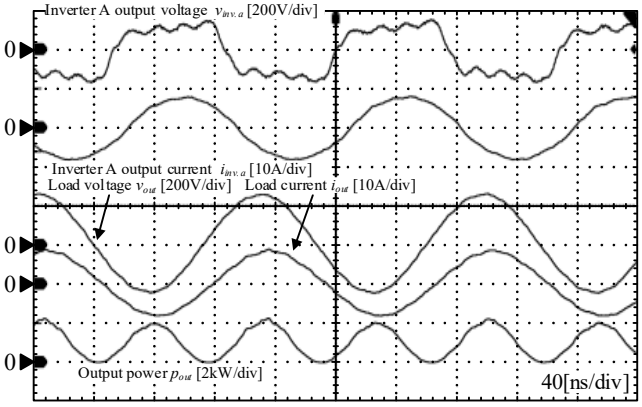
Fig. 7. Operation waveform of inverter output voltage, inverter output current and circulating currents

$$\alpha_{imb} = \frac{2\left(i_{inv.a} - i_{inv.b}\right)}{i_{inv.a} + i_{inv.b}} \qquad (2).$$

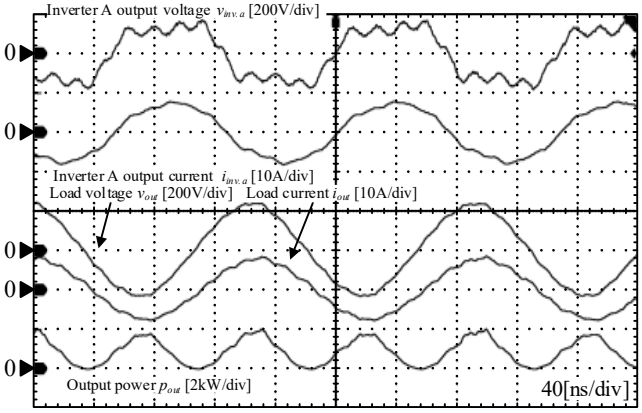
As shown in Fig. 7, the imbalance factors are 9.16% and 9.72%, respectively. In this experiment, the circulating current is evaluated as the difference between the inverter output currents; however, the component that should essentially be evaluated is the unbalanced component caused by voltage imbalance. Since the inverter current can be decomposed into balanced, unbalanced, and common-mode components, the circulating current defined as the current difference includes not only the unbalanced component but also the common-mode component. In the experimental results, the difference between the inverter currents, i.e., the circulating current, is almost the same for phase differences of 0° and 20°, at 538 mA and 533 mA, respectively. Although this result may appear to indicate that the circulating current does not change even when a phase difference is introduced, this is because the proposed balancer suppresses the increase in the unbalanced component. In other words, the unbalanced component would normally increase when a phase difference is introduced, and the current difference would consequently also increase; however, in the proposed method, this increase is suppressed because a high impedance is provided for the unbalanced component. As a result, the measured current difference is dominated primarily by the common-mode component and is therefore observed to remain almost constant regardless of the presence or absence of a phase difference. Therefore, these results indicate that the proposed balancer suppresses the generation of the unbalanced component and prevents an increase in the circulating current, thereby supporting the effectiveness of the proposed method.

Fig. 8 shows the output voltage and current of inverter a, the voltage and current of the load resistor, and their product, which corresponds to the load power, in the proposed system. Fig. 8(a) shows the operation when no phase difference exists between the inverters, whereas Fig. 8(b) shows the operation when a phase difference exists. When no phase difference is present, the load current is 5.77 A and the output power is 987 W. In contrast, when a phase difference exists, the load current is 5.38 A and the output power is 856 W, indicating a decrease in output power. This is because the balancer consumes reactive power to compensate for the imbalance in the inverter output voltages, thereby reducing the power factor. Here, the 20° phase difference in this experiment is set as a worst-case condition that considers wiring impedance, device variations, and gate driver delay. Under actual operating conditions, the phase difference is expected to be smaller than this value; therefore, the reduction in output power will be smaller than that observed in these results. Accordingly, considering the improvements in reliability due to circulating current suppression and the maintenance of current balance, the reduction in transmitted power caused by the proposed balancer is considered acceptable for practical use.

Fig. 9(a) and (b) show the gate–source voltage of the GaN FET, the inverter output voltage, the load voltage, and the load current of the proposed system under conditions with and without a phase difference between the inverter output voltages. The experimental results indicate that, under both operating conditions, the inverter output voltage rises approximately to the dc voltage before the plateau region of the gate–source voltage. This implies that the parasitic capacitances of the GaN FET are sufficiently discharged.

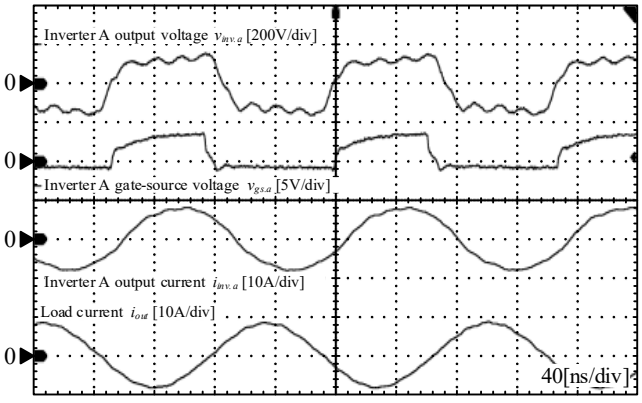


(a) without a phase difference of the proposed system.

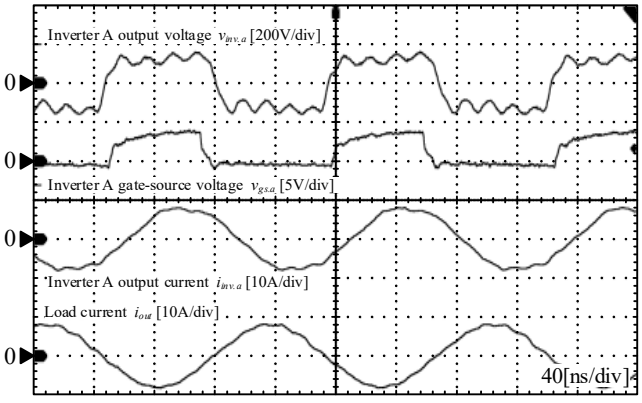


(b) with a phase difference of 20°

Fig 8. Input power and load power for the proposed system.



(a) without phases difference



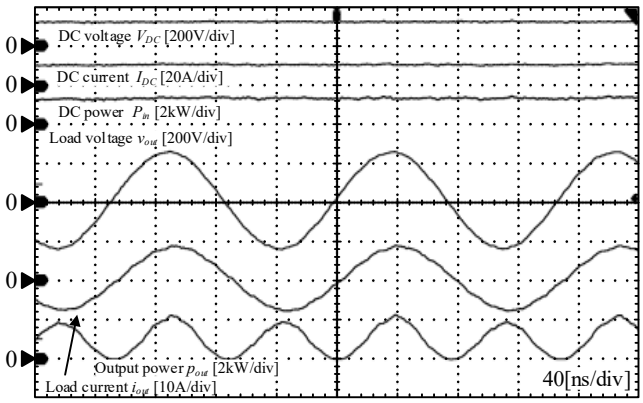
(b) with a phase difference of 20°

Fig 9. ZVS operation of the proposed system.

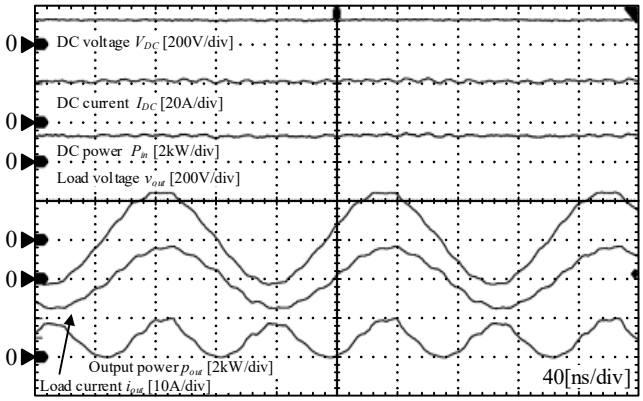
Although the waveforms suggest slightly incomplete discharge, the low device temperature during operation indicates that the switching loss is sufficiently reduced.

Figs. 10(a) and 10(b) show the DC input power and the load power under the conditions where no phase difference exists and where a phase difference exists between the inverter output voltages, respectively. The power is measured by acquiring the DC-side voltage and current, and the load-resistor voltage and current, using a differential probe and a current probe, and then calculating their product and average using the oscilloscope arithmetic function. From the waveforms, when no phase difference exists, the DC input power is 1.35 kW, and the load power is 964 W. When a phase difference exists, the DC input power is 1.30 kW, and the load power is 873 W. Therefore, the corresponding losses are 386 W and 427 W, respectively. In this system, the dominant sources of loss are the conduction losses of the resonant coil and the coupled inductor. The resonant coil is implemented as an air-core coil, resulting in a long conductor length and large loss. In addition, the number of turns of the coupled inductor is increased to obtain the required leakage inductance for transferring the rated power, thereby increasing the conduction loss. The experimental system is a prototype developed to verify current balancing and power transfer principles, and loss optimization has not been performed in the design of the passive components. In particular, the resonant coil has a long conductor length due to its air-core structure, and the coupled inductor has an increased number of turns to ensure the required leakage inductance, resulting in increased conduction losses. Therefore, the efficiency in these results corresponds to a pre-optimization value. In contrast, these losses are primarily attributed to conductor design and can be reduced by optimizing the number of turns and coupling coefficient of the coupled inductor, as well as by improving the conductor layout. Therefore, they are not inherent limitations of the proposed method, and efficiency can be improved through design optimization.

Fig. 11 shows the operating waveforms with and without the parallel resonant capacitor to confirm that the influence of the leakage inductance is suppressed. The measured waveforms are the inverter output voltage, inverter output current, load voltage, and load current. When the parallel capacitor is not used, ZVS is not achieved and the device temperature exceeds the allowable limit; therefore, the experiment is conducted with the dc voltage limited to 100 V. In this case, the inverter output current is 0.560 A, the load current is 0.872 A, and the load power is 21.24 W. This is because the leakage inductance increases the reactive component of the input impedance. In addition, since the inverter output current decreases significantly, the parasitic capacitance of the FET cannot be discharged, resulting in failure of ZVS. Consequently, significant ringing appears in both the voltage and current waveforms. In contrast, when the parallel resonant capacitor is used, the inverter output current is 4.20 A, the load current is 4.32 A, and the load power is 550 W. These results indicate that the proposed balancer with the parallel capacitor compensates for the leakage inductance and suppresses the reactive component of the input impedance, thereby improving the transferred power. Moreover, since sufficient current flows, ZVS is achieved. These results confirm that the proposed balancer compensates for the power factor degradation caused by leakage reactance and enables power transfer in the MHz band.

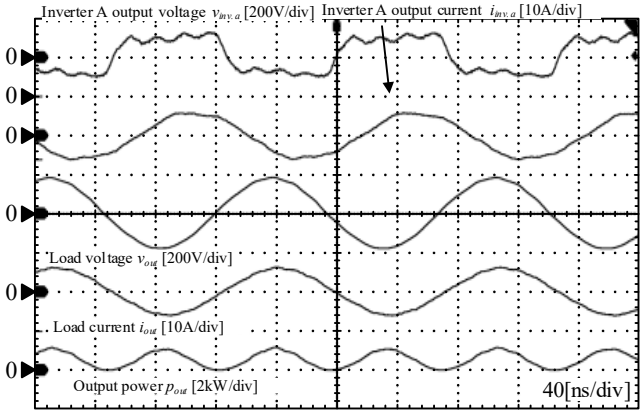


(a) without phase difference of the proposed system

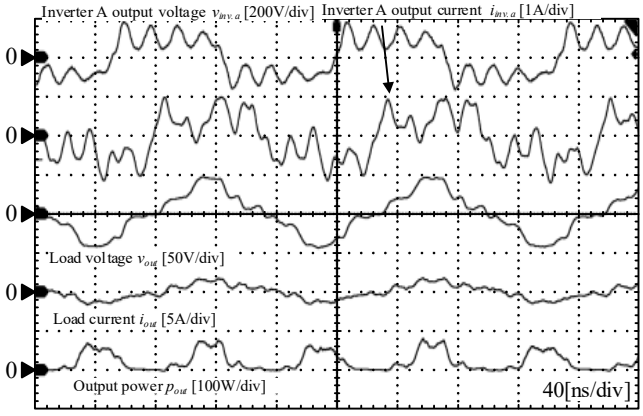


(b) with a phase difference of 20°

Fig 10. Measurement result of input power and output power.



(a) without phase difference of the proposed system



(b) Operation waveform with parallel resonant capacitor.

Fig.11 Comparison of operation using parallel resonant capacitors.

V. Conclusion

This paper proposes a configuration for parallel-connected MHz wireless power transfer (WPT) systems that maintains inverter current balance while compensating for the leakage inductance of coupled inductors. In the proposed circuit, resonant capacitors connected in parallel with the coupled inductors compensate for the leakage inductance. The effectiveness of the proposed balancer is experimentally verified using a 1-kW-class prototype operating at 6.78 MHz with a resonant load. Experimental results show that, at a phase difference of 0°, the output power is 964 W with an imbalance ratio of 9.16%, whereas at 20°, the output power is 873 W with an imbalance ratio of 9.72%. These results demonstrate that the proposed balancer achieves current balancing in MHz WPT systems while transferring power while mitigating power factor degradation due to leakage inductance. Future work includes the design of low-loss coupled inductors and transmission coils and experimental validation of WPT systems employing the proposed balancer.

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