Active Power Decoupling Using a Single Load-Side Inductor for Isolated AC-DC Converters in OBCs

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***Abstract*— This paper proposes an active power decoupling (APD) method for an isolated AC-DC converter without an additional inductor. The proposed method utilizes the load-side inductor to achieve APD and requires only one additional switch and a small buffer capacitor. An analytical expression for the duty ratio of the capacitor-voltage control is derived. Moreover, a modulation method to avoid DC magnetic bias in the transformer is considered. The proposed converter achieves power ripple suppression while maintaining power factor correction (PFC) on the AC side. Simulation results demonstrate APD operation in both grid-to-vehicle (G2V) and vehicle-to-grid (V2G) modes. A fundamental experiment using a 840 W prototype verifies the operation of the proposed APD control and modulation method. The experimental results show suppression effect of 100 Hz ripple component on the DC side to within 2.3 % while maintaining PFC operation.**

Keywords—Single Inductor; Power Decoupling; AC-DC converter; On-board charger; Bidirectional

I. INTRODUCTION

Electric vehicles (EVs) have become widely adopted as passenger vehicles in recent years. Because residential houses are typically supplied from a single-phase grid, on-board chargers (OBCs) require single-phase AC-DC conversion when EVs are charged at home. However, single-phase AC-DC conversion generates power pulsation on the DC side, which must be suppressed to extend battery lifespan [1-2].

Electrolytic capacitors have been widely used to suppress the power ripple at the DC output. Reference [3] shows an example of 11 kW single-phase AC-DC converter that employs a 2.43 mF DC-link capacitor. Nevertheless, limited lifetime and low reliability make them unsuitable for long-term use in OBCs. Therefore, ripple suppression without large electrolytic capacitors is required for single-phase grid-connected OBCs.

Active power decoupling (APD) has been widely studied as a method to suppress power ripple without electrolytic capacitors [3-24]. Although APD enables the use of smaller film or ceramic capacitors, conventional APD circuits typically require multiple additional switches and passive components such as inductors for current control [7-15], which increase the size of OBC.

On the other hand, AC-DC converters without additional components have been proposed [16-24]. References [16-18] focus on APD in multi-port converters. Moreover, [19-23] employ three-/single-phase compatible converters that utilize a redundant leg to achieve APD during single-phase operation. Although each converter in [16-23] achieves APD without additional components, circuit topologies become complex. Although [24] also presents an APD method without additional components, circuit parameter design becomes complex due to the trade-off between efficiency and power-density.

This paper proposes an APD method for an isolated AC-DC converter without an additional APD inductor. The proposed method utilizes the load-side inductor to achieve APD. Thus, the proposed method requires only one additional switch and a small buffer capacitor. The duty ratio required for APD is derived analytically. The effectiveness of the proposed method in suppressing power ripple is verified by simulation. Finally, power ripple suppression is demonstrated experimentally using an 840 W prototype.

II. PROPOSED CIRCUIT AND CONTROL

A. Features of the Proposed Circuit

Fig. 1 shows the configuration of the proposed AC-DC converter. The proposed circuit consists of a current source rectifier (CSR), an active buffer circuit [25], a full-bridge converter, and an output-stage inductor L_o. The output inductor L_o ensures that the load current I_{out} exhibits inductive

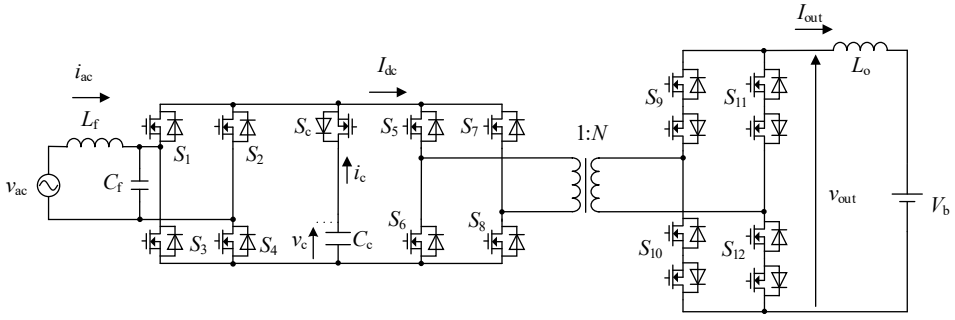


Fig. 1. Proposed single-phase isolated AC-DC converter with active power decoupling.

behavior. The proposed circuit utilizes the inductive characteristic of the load current I_{out} to control the buffer voltage v_c of the buffer capacitor C_c for APD. The output-stage inductor L_o is determined from the allowable switching ripple of the load current. The capacitance C_c is determined based on the required energy-buffer given in [25].

Table I compares the functional features of the proposed circuit with those of a conventional circuit. The conventional circuit consists of a PWM rectifier, a large-capacity electrolytic DC-link capacitor, and a phase-shift converter. The PWM rectifier controls the input current to achieve power factor correction (PFC). The large electrolytic DC-link capacitor suppresses power pulsation at the output of the AC-DC stage.

In contrast, the proposed circuit achieves APD using a small buffer capacitor. This feature enables the use of long-lifespan passive components such as ceramic capacitors or film capacitors. Thus, the proposed circuit provides higher reliability than the conventional circuit.

In terms of passive components, the conventional circuit employs inductors in both the AC-DC and DC-DC stages. In contrast, the proposed circuit requires only one inductor located on the load side. Furthermore, the conventional PWM rectifier cannot achieve zero-voltage switching (ZVS). Therefore, even if the conventional circuit uses a high-efficiency DC-DC converter, the overall system efficiency is limited by the switching losses in the AC-DC stage.

The proposed converter employs a CSR that enables synchronous rectification and reduces switching losses. However, the required voltage rating of the switching devices in the proposed circuit is higher. However, higher voltage-rated devices generally exhibit larger on-resistance. Thus, the proposed converter has higher conduction losses than the conventional converter.

TABLE I. Proposed circuit vs. Conventional circuit.

Item	Proposed	Conventional
Reliability	◎	△
Components	◎	○
Efficiency	○	○

B. Equivalent Circuit

Fig. 2 shows the equivalent circuit of the proposed converter. The secondary-side circuit in Fig. 1 is referred to the primary side, and the two full bridges around the transformer are omitted. The conversion formulas from the secondary side to the primary side are given in

$$I_{out}' = NI_{out} \quad \text{.....(1)},$$

$$V_b' = V_b / N \quad \text{.....(2)},$$

$$L_o' = L_o / N^2 \quad \text{.....(3)},$$

where N is the transformer turns ratio, I_{out} is the load current, I_{out}' is a referred load current, V_b is the load voltage, V_b' is a referred load voltage, L_o is the output inductance, and L_o' is a referred output inductance. The control method of the proposed circuit is analyzed using the equivalent circuit shown in Fig. 2 to simplify the analysis.

C. Load Current Control

Fig. 3 shows a block diagram of the load-current controller in the proposed circuit. A PI-controller is used to control the load current I_{out}'. Although the output voltage v_{out}' is the manipulated variable of the PI-controller, the actual output voltage v_{out} contains an error caused by the grid voltage v_{ac} and the buffer capacitor voltage v_c. The error voltage is defined as v_{error}. Thus, the bandwidth of the PI-controller is set much higher than the grid frequency and the buffer-voltage frequency to suppress the output voltage error v_{error}. The grid frequency is 50 Hz. Thus, the PI-controller bandwidth f_c is set to 2 kHz in this paper.

D. Control Strategy for Active Power Decoupling

The APD of the proposed circuit is controlled by charging and discharging the buffer capacitor C_c using the inductive load current I_{out}. Fig. 4 shows the charging and discharging current paths of the buffer capacitor C_c. The buffer capacitor C_c is charged and discharged through switch S_c. The full

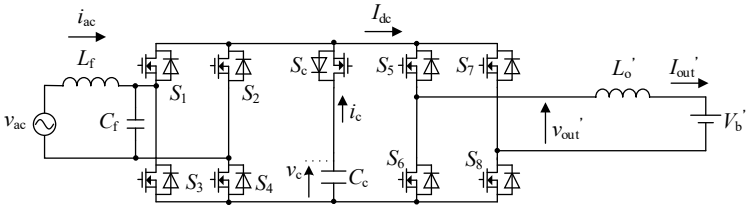


Fig. 2. Equivalent circuit of proposed circuit for control analysis.

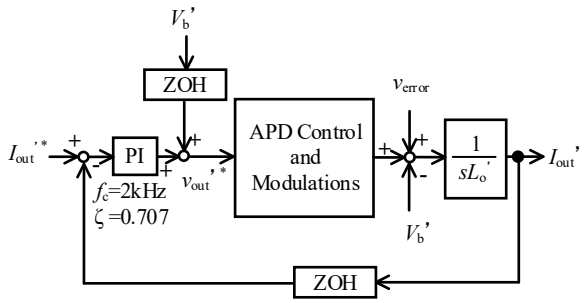


Fig. 3. Load-current controller with voltage error v_{error}.

bridge determines the charging mode and discharging mode by reversing the direction of I_{dc}.

Fig. 5 shows a block diagram of the APD controller. The buffer-voltage reference v_c^* is derived from the power balance of the active buffer circuit, as discussed in [25], and it is given by

$$v_c^* = \sqrt{\left(V_{cave}^*\right)^2 - \frac{p_{out}}{2\pi f_{ac} C_c}\sin 2\theta} \quad \text{..... (4),}$$

where V_{cave}^* is the average of capacitor-voltage reference, p_{out} is the output power, f_{ac} is the grid frequency, C_c is the capacitance of the buffer-capacitor, and θ is the grid phase angle. The average buffer voltage is controlled by a PI controller. Thus, the bandwidth of the voltage PI controller is set much lower than twice the grid frequency because the PI controller controls only the average value. Then, the bandwidth of the voltage PI controller is set to 10 Hz in this paper. In contrast, the AC component of the buffer voltage is controlled by feedforward control using the buffer-current command. Then, the buffer-current command of the feedforward control $i_{c\_FF}^*$ is given by

$$i_{c\_FF}^* = \frac{p_{out}}{v_c}\cos 2\theta \quad \text{..... (5).}$$

The sum of the PI-controller output and the feedforward term $i_{c\_FF}^*$ is used as the buffer current reference i_c^*, which is the manipulated variable of the capacitor-voltage controller. Each switch duty is calculated from the capacitor-current reference i_c^* by

$$d_c = \left|\frac{i_c^*}{\hat{I}_{dc}}\right| \quad \text{..... (6),}$$

$$d_{rec} = 2\alpha\left|\sin\theta\right| \quad \text{..... (7),}$$

$$d_z = 1 - d_{rec} - d_c \quad \text{..... (8),}$$

$$\alpha = \left(1 - d_{zmin}\right)\frac{V_{cave}^*}{2V_{cave}^* + V_{acp}} \quad \text{..... (9),}$$

where d_c is the on-duty of S_c, d_z is the duty during the zero-voltage period of the full-bridge output, d_{rec} is the duty during the conduction period of the diode bridge, $\hat{I}_{dc}$ is the estimated DC-link current, V_{acp} is the amplitude of the grid voltage, and d_{zmin} is the minimum value of d_z to prevent distortion of the grid current. The constant α represents the voltage-utilization ratio between the maximum output voltage v_{out} and the grid-voltage amplitude V_{acp}.

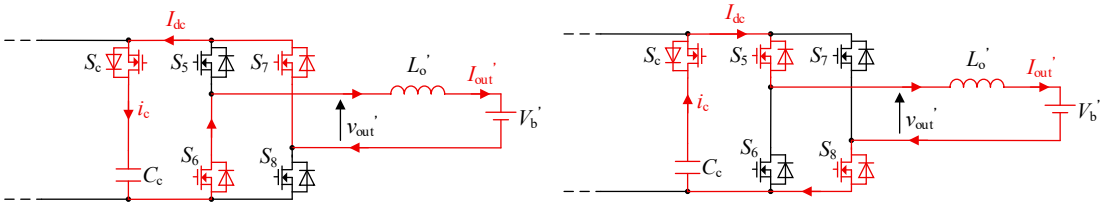
Fig. 6 shows the normalization and modulation diagram of proposed circuit, which performs modulation for APD and output-voltage PWM. Output-voltage PWM is performed by unipolar modulation using a trapezoidal carrier. Then, the estimated DC-link voltage $\hat{v}_{dc}$ is calculated as the average value excluding the d_z period when the full bridge does not contribute to the output voltage. Then, the estimated DC-link voltage $\hat{v}_{dc}$ is given by

$$\hat{v}_{dc} = \mathrm{sign}(i_c) d_c v_c + d_{rec}\left|v_{ac}\right| \quad \text{..... (10),}$$

$$\hat{v}_{dc} = \left(\mathrm{sign}(i_c) d_c + d_{rec}\right) v_c \quad \text{..... (11).}$$

The duty ratio of the output-voltage d is calculated by output voltage reference v_{out}^* and estimated DC-link voltage $\hat{v}_{dc}$.

During V2G operation, CSR switching is suspended near the zero crossing of the input voltage to avoid short-circuiting the filter capacitor C_f. In this condition, (11) is used to calculate $\hat{v}_{dc}$. Then, the load current flows through and charges the buffer capacitor instead of AC voltage source. In other conditions, (10) is used to calculate $\hat{v}_{dc}$.



(a) charging mode (b) discharging mode

Fig. 4. Current path of buffer capacitor.

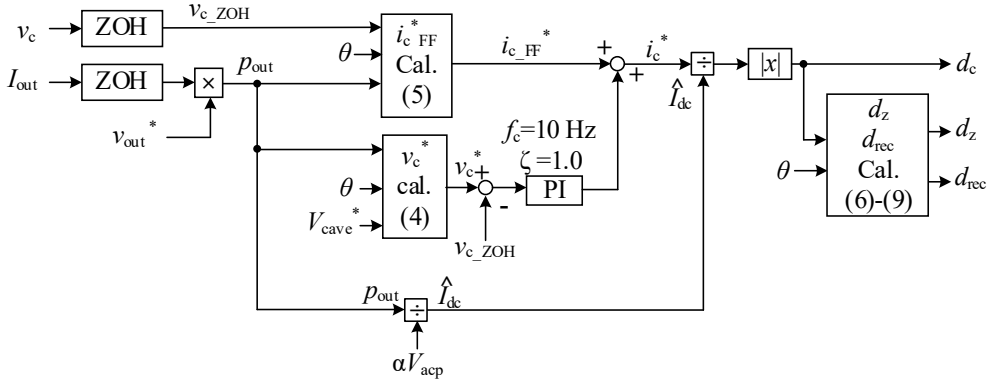


Fig. 5. Control diagram of buffer capacitor voltage for proposed APD.

Fig. 7 shows the modulation scheme for APD and output voltage PWM. The gate signals of S_c and S_{rec} are generated by comparing d_c and d_{rec} with a triangular carrier. In contrast, the gate signals S_5-S_8 in the equivalent circuit are generated by unipolar modulation using the trapezoidal carrier and the calculated duty ratios.

The output voltage of the transformer is generated by combining the capacitor voltage and the rectified voltage. Each duty ratios d_c and d_{rec} determines the application interval of each voltage modes. In addition, a zero-voltage interval of the full bridge d_z, which does not contribute to the output voltage, is introduced.

Then, a trapezoidal carrier is employed to represent the time structure in the modulation. The trapezoidal carrier is generated using the rising edges of S_c and S_{rec} as triggers. The rising interval of the carrier corresponds to the on-duration of S_c, and the falling interval corresponds to the on-duration of S_{rec}. The flat region of the carrier represents the zero-voltage interval d_z. The PWM operation of the output voltage is performed by comparing the output-voltage reference with the carrier. The same duty-generation principle, which is same as the conventional triangular-carrier PWM, is applied. The time allocation of each voltage source is embedded in the carrier waveform, enabling the simultaneous realization of voltage selection and output-voltage PWM. Therefore, APD is achieved without complex modulation schemes.

In contrast, the output voltage polarity of the full bridge is reversed to prevent DC bias in the transformer. Then, the gate signals of the full bridge are generated by swapping the gate signals of each leg in the equivalent circuit when base carrier is 1. Then, the load current is constant. Moreover, the transformer current direction is determined by the secondary full bridge. Thus, the current direction of C_c is controlled by the secondary bridge.

TABLE II. Simulation conditions of proposed circuit.

Parameters	Symbol	Value
Input Voltage	V_{ac}	200 V
Grid Frequency	f_{ac}	50 Hz
Output Voltage	V_b	400 V
Active Buffer Capacitor	C_c	195 μF
Average Capacitor Voltage Reference	V_{cave}^*	450 V
Output Inductor	L_o	1429 μH
Transformer Turn Ratio	N	5.0
Transformer Magnetizing Inductance	L_M	1.0 mH
Sampling Frequency	f_{sample}	20 kHz
Carrier Frequency	f_{sw}	100 kHz
Filter Capacitor Capacitance	C_f	29 μF
Filter Inductor Inductance	L_f	54 μH

III. Simulation Results of Proposed Circuit

Table II shows the simulation conditions. The rated output power is 7 kW. The cutoff frequency of the input filter is designed to be 1/10 of the switching frequency. The output inductance L_o is designed based on the load-current ripple. The capacitance of the active buffer capacitor C_c is 195 μF, which is less than 1/10 of the capacitance used in the conventional circuit.

Fig. 8 shows the simulation results of the proposed circuit in grid-to-vehicle operation. Fig. 8(a) shows the input voltage. Fig. 8(b) shows that the grid current is controlled to be sinusoidal. The power factor on the grid side is almost unity by the current control of the proposed circuit. Fig. 8(c) shows that the 100 Hz ripple component of the load current is suppressed. The capacitor-voltage control of the proposed

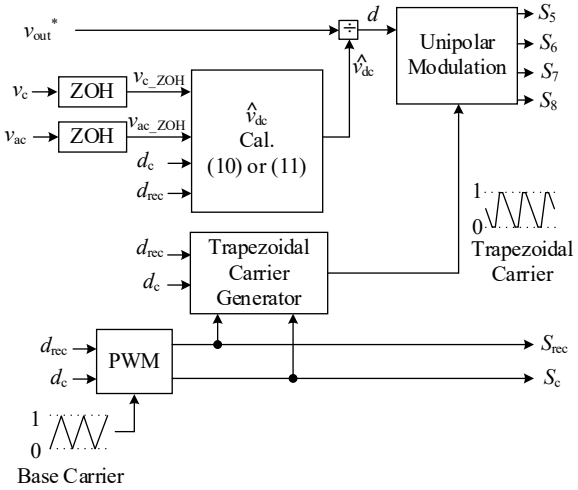


Fig. 6. Normalization and modulation scheme for APD and output-voltage PWM.

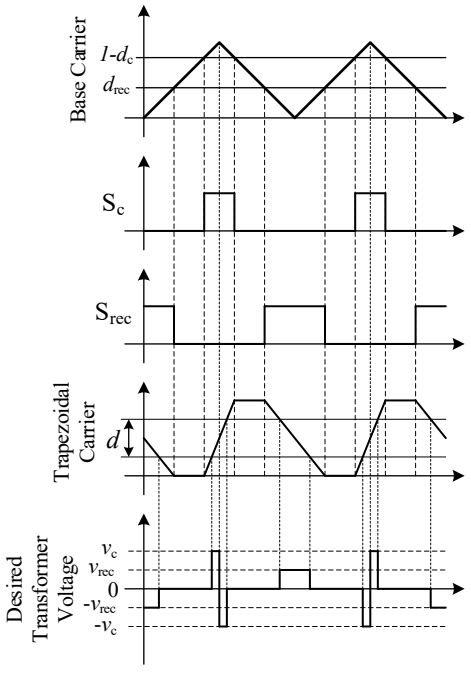
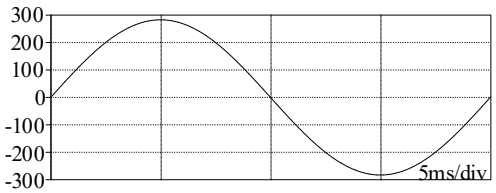
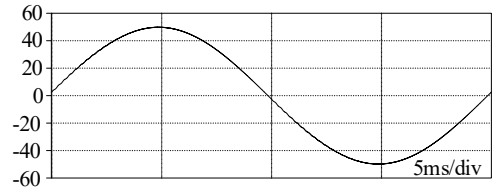


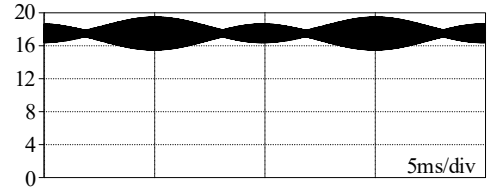
Fig. 7. Modulation scheme for APD operation and desired transformer voltage.



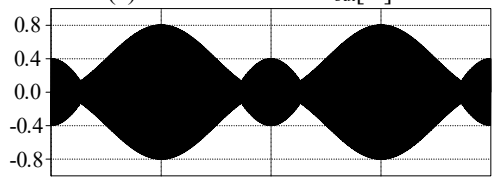
(a)Grid Voltage v_{ac}[V]



(b)Grid Current i_{ac}[A]

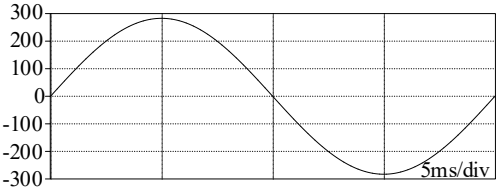


(c)DC Load current I_{out}[A]

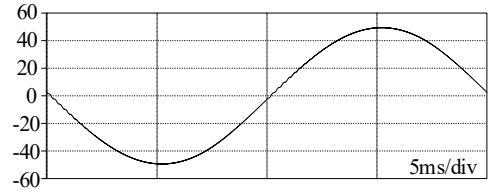


(d)Transformer Magnetizing Current[A]

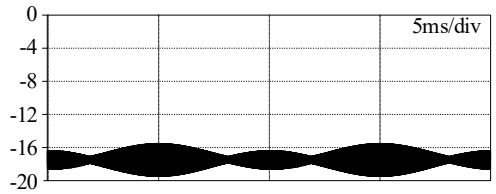
Fig. 8. Simulation result of Grid to Vehicle operation.



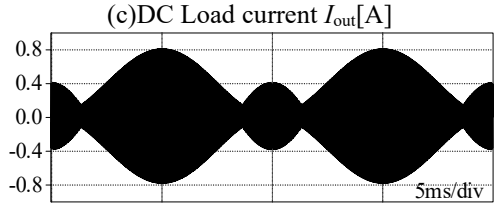
(a)Grid Voltage v_{ac}[V]



(b)Grid Current i_{ac}[A]



(c)DC Load current I_{out}[A]



(d)Transformer Magnetizing Current[A]

Fig. 9. Simulation result of Vehicle to Grid operation.

circuit achieves APD. Then, the average load current is maintained at the reference value of 17.5 A by the load-current controller. Moreover, the amplitude of the 100 Hz ripple component of the load current is 18 mA. Fig. 8(d) shows the transformer magnetizing current. The average magnetizing current is almost zero. Thus, Fig. 8(d) indicates that the transformer is not biased with the proposed modulation.

Fig. 9 shows the simulation results of the proposed circuit in vehicle-to-grid operation. Fig. 9(a) shows the input voltage. Fig. 9(b) shows that the grid current is controlled to be sinusoidal. The power factor on the grid side is almost unity by the current control of the proposed circuit. Moreover, Fig. 9(c) shows suppression of the 100 Hz ripple component of the load current. The capacitor-voltage control of the proposed circuit achieves APD. The average load current is maintained at the reference value of -17.5 A by the load-current controller. Then, the 100 Hz ripple component of the load current is 235-mA. Fig. 9(d) shows the transformer magnetizing current. The average magnetizing current is almost zero. Thus, DC bias does not occur in the transformer.

IV. Experiment Results of Proposed Circuit

The validity of the proposed circuit and control method is verified through a fundamental experiment using a prototype circuit. The voltage source in Fig. 2 is replaced with a current-source load, that is used to verify the operation of the APD controller and the modulation method. Although the simulation is conducted at the rated condition of 7 kW, the experimental validation is performed at 840 W due to laboratory constraints. The scalability of the proposed method is ensured by circuit parameter design and the selection of switching devices with suitable current ratings. The load current is not controlled by PI controller in the experiment. The load in the fundamental experiment consists of a resistor and an inductor. The load parameters are selected to make a load current behave as a current source. Since the battery behaves approximately as a constant-voltage load, the output-voltage reference generated by the current controller becomes almost constant in steady state. Therefore, the fundamental validity of the proposed APD control can be verified by applying a constant output-voltage reference to a current-source load that draws an approximately constant current.

Fig. 10 shows the experimental results in grid-to-vehicle operation. The grid current i_{ac} is controlled to be sinusoidal with switching ripple. The ripple amplitude depends on the parameters of AC filter. Although the reference of the output voltage v_{out}^* is constant, the load current contains ripple components caused by the switching ripple. Then, the amplitude of DC component of the load current is 10.15 A and output DC power at the load resistor is 840 W.

Fig. 11 shows the amplitudes of the harmonic components in the load current. Each component is normalized by the amplitude of the DC component. The 100 Hz ripple component of the load current is 235 mA, corresponding to 2.3% of the DC component. Thus, the proposed circuit and APD method suppress the 100 Hz ripple component to within 2.3% with 840 W single phase AC-DC conversion in the fundamental experiment.

V. Conclusion

This paper proposed an APD method and its control scheme for an isolated AC-DC converter without an additional inductor. The proposed method utilized the load-

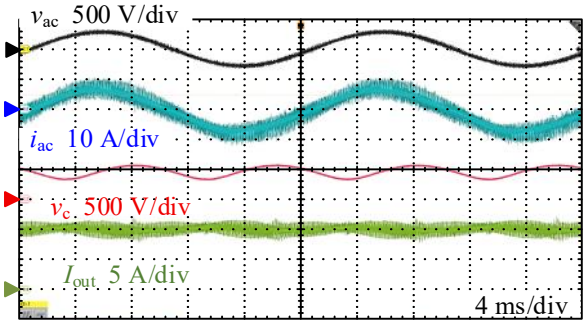


Fig. 10. Operation waveforms on prototype circuit.

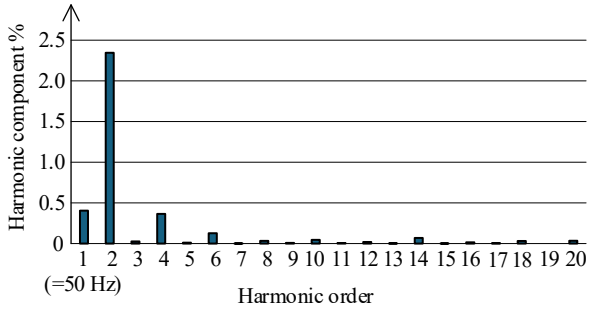


Fig. 11. Output current frequency analysis result.

side inductor to achieve APD and required only one additional switch and a small buffer capacitor. An analytical expression of the duty ratio for capacitor-voltage control was derived, and a control structure combining the capacitor-voltage control and load-current control was established.

Simulation results showed that the proposed circuit achieved power ripple suppression in both grid-to-vehicle and vehicle-to-grid operations while maintaining PFC operation. The magnetizing current of the transformer had an average value close to zero, and no DC bias occurred in the transformer by the proposed modulation.

Experimental results using 840 W prototype verified the fundamental operation of the proposed APD control and modulation method. Finally, the load current ripple is suppressed to 2.3% of DC component, as verified by the prototype experiment.

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