Broadband Control for Virtual Impedance Circuits Based on a Model-Matching Approach

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***Abstract*—This paper proposes a control design method for LCL-based virtual impedance circuits. Virtual impedance circuits emulate various impedance characteristics. With the recent progress of wide-bandgap devices such as GaN-HEMTs, high-frequency switching operation has become feasible. However, large-capacity power converters such as grid-tied inverters are typically operated at switching frequencies of only several kilohertz. Under such conditions, broadband virtual reactance emulation is difficult, particularly in LCL-based circuits whose plant order becomes higher under digital control. The proposed control expands the emulation bandwidth compared with the conventional method. Experimental results are presented for an input frequency corresponding to 10% of the switching frequency. At this frequency, the proposed control suppresses the phase rotation by 57% compared with the conventional method. The results indicate that the proposed method can maintain virtual inductive behavior at a lower switching frequency than that required by the conventional method, although some emulation error remains in the high-frequency region.**

Keywords—Digital control, State-feedback, Multirate control, Virtual impedance circuits

I. Introduction

Virtual impedance circuits are impedance emulators driven by switching devices. In recent years, large-capacity power converters, such as inverters and rectifiers, have increased in demand due to stringent efficiency requirements. Generally, the switching frequencies of these converters are set to several kHz or lower to reduce switching losses. In that case, the low-frequency component becomes significant in the low-switching frequency. Passive power filters are always employed to mitigate harmonic currents or voltages. However, these passive power filters consist of bulky inductors and capacitors. Moreover, electrolytic capacitors are inherently less durable than other components.

To overcome these problems, active power filters (APFs) are proposed in [1-2]. These additional power converters inject a compensation current into the grid to cancel the harmonic current generated by the main power converters. However, the compensation current of APFs may damage static capacitors connected to the grid side if the impedance between the main converters and the APFs is relatively high. Moreover, the phase-lag restriction in APFs is relatively strict (60 degrees). This means that it is difficult to reduce the switching frequency of APFs. Furthermore, alternatives to the electrolytic capacitors are also proposed as active capacitors in [3]. Active capacitors achieve long-lifetime capacitance, but their target is only capacitors.

Reference [4] proposes an impedance emulator. This circuit emulates a reactance by controlling the input current in response to the input voltage. However, the application of these emulators was limited, such as the cancellation of wiring inductance due to their low switching frequency.

The state-feedback-based approach is considered a control strategy for power converters, including resonance damping, as shown in [8]. Generally, the current control bandwidth cannot exceed the natural resonance frequency of the LCL structure, as the controller excites the resonance. However, the state-feedback approach can ensure that the system poles are stable, thereby effectively suppressing resonance. This feature has an advantage when the upper limit on switching frequency is restricted.

In this paper, a control method for general-purpose two-terminal virtual impedance circuits is proposed. To suppress the input-current ripple, the virtual impedance circuit is configured with an LCL filter. As a result, the plant becomes higher order, which makes broadband virtual impedance emulation more challenging in digital control. The emulation bandwidth of conventional virtual impedance circuits is limited by the switching frequency and the group-delay characteristic of the current control loop. This limitation becomes significant when the target frequency approaches the switching frequency. To address this issue, this paper introduces a state-feedback-based control framework with an external compensator derived from a model-matching approach. The proposed method shapes the transfer characteristic from the input voltage to the input current so that the circuit behaves approximately as a discrete integrator followed by a low-pass filter. As a result, the emulation bandwidth can be extended without requiring an excessively high switching frequency.

The main contribution of this paper is a control strategy for virtual impedance circuits that utilizes the input voltage as a disturbance signal. When this control is applied, virtual impedance circuits behave approximately as a discrete integrator followed by a low-pass filter. The proposed method is expected to reduce the switching losses of the virtual impedance circuit while maintaining a comparable emulation bandwidth.

II. Circuit and Control Structure

A. Circuit configurations

Figure 1 shows an application example of the virtual impedance circuit. In this case, the virtual impedance circuit behaves as an inductance. The filter cutoff frequency is set freely without swapping components, since the inductance

emulated by the virtual impedance circuit can be artificially adjusted.

Figure 2 shows the circuit configuration for implementing the virtual impedance. The circuit consists of an LC filter, an internal inductor L, a full-bridge inverter, and a bus voltage source. The LC filter is employed to suppress the switching ripple. The internal inductor is used to regulate the input current I_{in}. The inverter and bus voltage source act as the variable voltage source for the control input.

If a capacitor is used as the DC bus voltage source, most of the energy associated with the emulated impedance is stored in the bus capacitor. Therefore, the power density of the virtual impedance circuit is expected to be higher than that of a conventional inductor with the same inductance because the energy density of capacitors is generally higher than that of inductors. For simplicity, a constant voltage source is used as the bus voltage source in this paper.

The plant model in continuous-time state-space form is given by (1) and (2).

$$\frac{d}{dt}\mathbf{x} = \mathbf{A}_C\mathbf{x} + \mathbf{b}_C u + \mathbf{b}_{Cdist} w \quad \cdots\cdots (1)$$

$$y = \mathbf{c}_C\mathbf{x} \quad \cdots\cdots (2)$$

where state quantity $\boldsymbol{x}$, control input u, disturbance w, and control output y are expressed as in (3).

$$\mathbf{x} = \begin{bmatrix} V_C \\ I_{in} \\ I_L \end{bmatrix}, u = V_{conv}, w = V_{in}, y = I_{in} \quad \cdots\cdots (3)$$

The coefficient matrices $\boldsymbol{A}_C$, $\boldsymbol{b}_C$, $\boldsymbol{b}_{dist}$, and $\boldsymbol{c}_C$ are expressed as in (4).

$$\mathbf{A}_C = \begin{bmatrix} 0 & \frac{1}{C_f} & -\frac{1}{C_f} \\ -\frac{1}{L_f} & 0 & 0 \\ \frac{1}{L} & 0 & 0 \end{bmatrix}, \mathbf{b}_C = \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L} \end{bmatrix}, \mathbf{b}_{Cdist} = \begin{bmatrix} 0 \\ \frac{1}{L_f} \\ 0 \end{bmatrix}, \mathbf{c}_C = [0 \quad 1 \quad 0] \quad \cdots\cdots (4)$$

B. *Conventional control*

Figure 3 shows the conventional control system for virtual impedance circuits. According to this control, the command value for the current control is calculated in the analog integrator. The input current I_{in} follows the calculated current command owing to the current control system. However, the delay of the current control system cannot be smaller than twice the control period. This is because the transfer characteristic from the input voltage V_{in} to the input current I_{in} is strictly proper.

In case the continuous LCL plant is discretized, assuming zero-order hold, the numerator order of the transfer function becomes 2. On the other hand, the order of the denominator is 3 because the number of poles is preserved between the continuous time region and the discretized time region. Therefore, the relative order of the plant is 1 under natural conditions. However, there is a one-sample delay from detection and control calculation to PWM output. This increases the relative order of the plant. A higher relative order of the plant leads to slower tracking performance. For an LCL plant, the relative order is 2 in the standard digital control. In this case, the fastest settling of input current becomes twice the control period. To achieve this deadbeat response with a

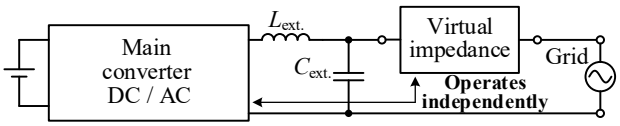


Fig.1. Implementation of a virtual impedance circuit for a switching filter.

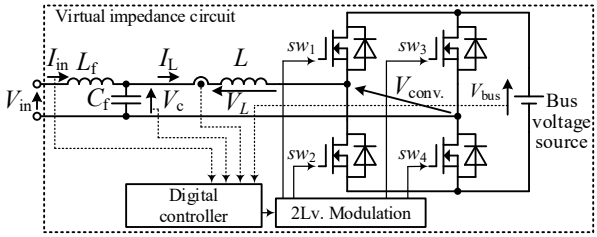


Fig. 2. Circuit configuration of a virtual impedance circuit.

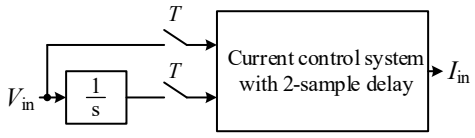


Fig.3. Control system of the conventional control

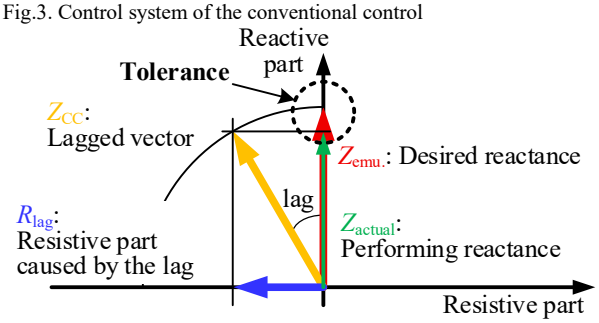


Fig.4. Relationship between the desired reactance and performing reactance.

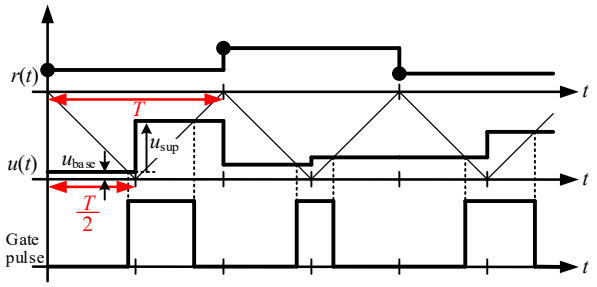


Fig.5. Gate pulse generation in a multirate system.

2-sample delay, zero-magnitude error tracking control (ZMETC), proposed in [11], is employed.

This fixed delay is known as the group delay characteristic. This effect becomes significant as the input voltage frequency approaches that of the virtual impedance circuit.

C. *Cause of the bandwidth limitation*

Figure 4 shows the phasor diagram. The red vector shows the desired reactance emulated by the virtual impedance circuit. The yellow vector is the lagged vector by conventional control. As mentioned previously, conventional control uses the current control system with a group-delay characteristic. This group delay causes a phase shift at the yellow vector. The green vector indicates the actual reactance emulated by the virtual impedance circuit. The blue vector indicates the active power caused by the lag. The active power in the virtual impedance circuit causes the bus voltage to increase or decrease when the capacitor is used as the bus voltage source.

Even when a constant-voltage source is used as the bus voltage source, emulation accuracy deteriorates due to the lag.

III. Control Design.

A. Multirate discretization

Figure 5 shows triangular-wave-based gate pulse generation. A discrete-time plant model is required for digital control. Multirate PWM is employed to obtain robustness.

The switching frequency does not increase even when the duty command is changed once at the midpoint of the control period. Multirate discretization based on this operation is carried out by calculating (5) and (6).

$$\mathbf{A}_P = e^{\mathbf{A}_C T}, \mathbf{b}_{Pbase} = \int_0^T e^{\mathbf{A}_C \tau} \mathbf{b}_C d\tau, \mathbf{b}_{Psup} = \int_0^{\frac{1}{2}T} e^{\mathbf{A}_C \tau} \mathbf{b}_C d\tau, \mathbf{c}_P = \mathbf{c}_C \quad (5)$$

$$\mathbf{b}_{Pdist} = \int_0^T e^{\mathbf{A}_C \tau} \mathbf{b}_{Cdist} d\tau \quad (6)$$

where T is the sampling period. The discretized matrix and vectors are given by (7), (8), and (9), respectively.

$$\mathbf{A}_P = \begin{bmatrix} \cos\omega T & -\omega\frac{LL_f}{L+L_f}\sin\omega T & \omega\frac{LL_f}{L+L_f}\sin\omega T \\ \frac{1}{\omega L_f}\sin\omega T & \frac{L_f}{L+L_f}\left(1+\frac{L}{L_f}\cos\omega T\right) & \frac{L}{L+L_f}(1-\cos\omega T) \\ -\frac{1}{\omega L}\sin\omega T & \frac{L_f}{L+L_f}(1-\cos\omega T) & \frac{L}{L+L_f}\left(1+\frac{L_f}{L}\cos\omega T\right) \end{bmatrix} \quad (7)$$

$$\mathbf{b}_{Pbase} = \frac{1}{L+L_f}\begin{bmatrix} -L_f(\cos\omega T - 1) \\ -\left(T - \frac{1}{\omega}\sin\omega T\right) \\ -\left(T + \frac{1}{\omega}\cdot\frac{L_f}{L}\sin\omega T\right) \end{bmatrix}, \mathbf{b}_{Psup} = \frac{1}{L+L_f}\begin{bmatrix} -L_f\left(\cos\frac{1}{2}\omega T - 1\right) \\ -\left(\frac{1}{2}T - \frac{1}{\omega}\sin\frac{1}{2}\omega T\right) \\ -\left(\frac{1}{2}T + \frac{1}{\omega}\cdot\frac{L_f}{L}\sin\frac{1}{2}\omega T\right) \end{bmatrix} \quad (8)$$

$$\mathbf{b}_{Pdist} = \frac{1}{L+L_f}\begin{bmatrix} -L(\cos\omega T - 1) \\ T + \frac{1}{\omega}\cdot\frac{L_f}{L}\sin\omega T \\ T - \frac{1}{\omega}\sin\omega T \end{bmatrix} \quad (9)$$

where ω is the natural resonant frequency of this plant expressed in (10).

$$\omega = \sqrt{\frac{1}{C_f}\left(\frac{1}{L_f} + \frac{1}{L}\right)} \quad (10)$$

There is one sample delay in the voltage output. To obtain an accurate plant model for control, the previous value of the control input $\boldsymbol{u}$[k-1] is included in the state quantity vector. Finally, the extended plant model is expressed as in (11) and (12).

$$\mathbf{x}[k+1] = \mathbf{A}_D\mathbf{x}[k] + \mathbf{B}_D\mathbf{u}[k] + \mathbf{b}_{Ddist}w[k] \quad (11)$$

$$y[k] = \mathbf{c}_D\mathbf{x}[k] \quad (12)$$

where the state quantity vector $\boldsymbol{x}$ is re-defined as in (13).

$$\mathbf{x} = \begin{bmatrix} V_C[k] \\ I_{in}[k] \\ I_L[k] \\ \mathbf{u}[k-1] \end{bmatrix} = \begin{bmatrix} V_C[k] \\ I_{in}[k] \\ I_L[k] \\ u_{\text{base}}[k-1] \\ u_{\text{sup}}[k-1] \end{bmatrix} \quad (13)$$

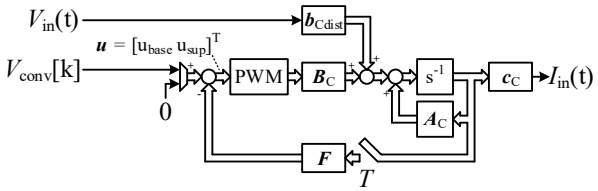


Fig.6. Structure of the state feedback for stabilization.

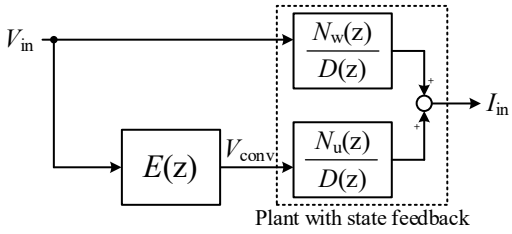


Fig. 7. Introduction of the external compensator.

Finally, $\boldsymbol{A}_{\text{D}}$, $\boldsymbol{B}_{\text{D}}$, $\boldsymbol{b}_{\text{Ddist}}$, and $\boldsymbol{c}_{\text{D}}$ are expressed in (14) and (15), respectively.

$$\mathbf{A}_D = \begin{bmatrix} \mathbf{A}_P & \mathbf{b}_{\text{Pbase}} & \mathbf{b}_{P\text{sup}} \\ \mathbf{0}_{2\times3} & \mathbf{0}_{2\times1} & \mathbf{0}_{2\times1} \end{bmatrix} \quad (14)$$

$$\mathbf{B}_D = \begin{bmatrix} \mathbf{0}_{3\times2} \\ \mathbf{I}_{2\times2} \end{bmatrix}, \mathbf{b}_{Ddist} = \begin{bmatrix} \mathbf{b}_{Pdist} \\ \mathbf{0}_{2\times1} \end{bmatrix}, \mathbf{c}_D = \begin{bmatrix} \mathbf{c}_P & \mathbf{0}_{1\times2} \end{bmatrix} \quad (15)$$

B. State feedback

Figure 6 shows the state feedback structure. As mentioned previously, in the virtual impedance circuit, group delay characteristics should be avoided. The Bessel characteristic is employed for its minimum group delay. Here, the 5th order case is considered because the order of the target plant is 5. The 5th-order inverse Bessel polynomial θ_5(x) is expressed in (16).

$$\theta_5(x) = \sum_{k=0}^{5}\frac{(5+k)!}{(5-k)!k!}\cdot\frac{x^{5-k}}{2^k} = x^5 + 15x^4 + 105x^3 + 420x^2 + 945x + 945 \quad (16)$$

The transfer function of the low-pass filter with Bessel characteristics is given in (17).

$$H_5(s) = \frac{\theta_5(0)}{\theta_5\left(\frac{s}{\omega_{\text{cut}}}\right)} = \frac{945\omega_{\text{cut}}^5}{s^5 + 15\omega_{\text{cut}}s^4 + 105\omega_{\text{cut}}^2s^3 + 420\omega_{\text{cut}}^3s^2 + 945\omega_{\text{cut}}^4s + 945\omega_{\text{cut}}^5} \quad (17)$$

Poles in the continuous time region of the Bessel characteristic are given as roots of the denominator of (17). The relationship between poles in the continuous time region p_{C} and in the discretized time region p_{D} is given in (18).

$$p_{\text{D}} = e^{p_{\text{C}}T} \quad (18)$$

Poles of the plant are specified by applying the feedback coefficient matrix $\boldsymbol{F}$. $\boldsymbol{F}$ is determined so that the eigenvalues of the modified state transient matrix $\boldsymbol{A}_{\text{mod}}$, given in (19), are the desired poles.

$$\mathbf{A}_{\text{mod}} = \mathbf{A}_{\text{D}} - \mathbf{B}_{\text{D}}\mathbf{F} \quad (19)$$

C. Design of the external compensator E(z)

Figure 7 shows the introduction of the external compensator E(z). This compensator is placed between the input voltage V_{in} and the converter voltage V_{conv}. The

denominator of the state-feedback-modified plant $D(z)$ is common because the poles are shared across all paths.

The main purpose of applying $E(z)$ is to add an immovable integrator pole. An integrator pole can also be placed initially via state feedback; however, parameter errors or model mismatches may exist in the actual circuit. These errors cause pole misalignment, which can make the plant unstable. For this reason, an artificial integrator pole is required for the control design of virtual impedance circuits.

As shown in Figure 7, the transfer function from V_{in} to I_{in} is given by (20).

$$G_{mod}(z)=\frac{I_{in}}{V_{in}}=\frac{N_w(z)}{D(z)}+E(z)\cdot\frac{N_u(z)}{D(z)} \quad \text{.....(20)}$$

The target transfer function is the cascade of a discrete integrator with integration gain and a low-pass filter with a Bessel characteristic. By applying state feedback, the plant is already modified to a Bessel filter.

The transfer function from control input to the output has discretization zeros due to the calculation delay. Furthermore, one of the zeros can become unstable. If the plant has an unstable zero, the inverse system of the plant is unavailable for a feedforward compensator to preserve internal stability. This problem is well known and has been considered in digital control theory; for example, reference [11] proposes a feedforward compensator based on a symmetric zero (or symmetric pole placement). The symmetric zero, z_{sym}, is the stable zero, calculated from an unstable zero and given by (21).

$$z_{sym}=\frac{1}{z_{unstable}} \quad \text{.....(21)}$$

where $z_{unstable}$ is the unstable zero. The reason why z_{sym} becomes a stable zero is that the norm of the unstable zero exceeds 1 from the definition. By introducing z_{sym} to the feedforward compensator instead of the unstable zero, a quasi-inverse of the plant with stable roots is obtained.

Based on this approach, the transfer function of the compensator $E(z)$ is given by (22).

$$E(z)=\frac{K}{z-1}\cdot\frac{N_w(z)}{N_u'(z)}=K\cdot\frac{N_w(z)}{(z-1)\cdot\prod_{i=1}^{n_{stable}}(z-q_i)\cdot\prod_{i=1}^{n_{unstable}}\left(z-\frac{1}{r_i}\right)} \quad \text{.....(22)}$$

where N_u'(z) is the polynomial which has stable zeros and symmetric zeros as its roots, K is the arbitrary gain, q_i is the i^{th} stable zero, r_i is the i^{th} unstable zero, n_{stable} is the number of stable zeros, and $n_{unstable}$ is the number of unstable zeros. That is, the stable zeros are canceled directly, whereas each unstable zero is replaced by a pole located at its symmetric position inside the unit circle.

Assuming that the dynamics of the unstable zero in the plant and the pole based on the symmetric zero in the feedforward compensator are cancelled out, the transfer function of the cascade of the compensator $E(z)$ and the plant is approximated as (23) under nominal modeling conditions.

$$E(z)\cdot\frac{N_u(z)}{D(z)}\approx\frac{K}{z-1}\cdot\frac{N_w(z)}{D(z)} \quad \text{.....(23)}$$

Therefore, the transfer function of the entire system $G_{mod}(z)$ is given by (24).

$$G_{mod}(z)=\frac{I_{in}}{V_{in}}\approx\frac{z-1+K}{z-1}\cdot\frac{N_w(z)}{D(z)} \quad \text{..... (24)}$$

The integral gain of the entire system is required to determine the gain K. Normally, in a stable system, the steady gain is calculated by substituting 1 for z in the transfer function. However, in virtual impedance circuits, there is a pole at z = 1. Therefore, the residue of z = 1 is considered as an integral gain. The integral gain G_{int} is calculated by (25).

$$G_{int}=\frac{1}{L_{emu.}}=\lim_{z\to1}\left\{\frac{z-1}{T}\cdot G_{mod}(z)\right\} \quad \text{..... (25)}$$

where $L_{emu.}$ is the desired inductance.

The integral gain, G_{int}, represents the gain of the plant relative to that of a unit discrete integrator.

Finally, the gain K is determined from the desired inductance by calculating (26).

$$K=\frac{T}{L_{emu.}}\cdot\left\{\frac{D(z)}{N_w(z)}\cdot\frac{N_u(z)}{N_u'(z)}\bigg|_{z=1}\right\}^{-1} \quad \text{..... (26)}$$

IV. Simulation Results

A. Gain derivation

Table 1 shows the circuit parameters for simulation and experiment. All further analysis is based on these parameters. In this condition, the resonance frequency of the LCL structure is 1729 Hz, as given in (10).

The state-feedback coefficient vector $\boldsymbol{F}$ is designed so that the poles of the system match those of the Bessel filter in (27).

$$\mathbf{F}=\begin{bmatrix}-0.367 & -9.36 & -10.0 & 1.67 & 0.915\\ -0.558 & 8.04 & 14.3 & -1.97 & -1.06\end{bmatrix} \quad \text{..... (27)}$$

The cutoff frequency of the LPF is set to 1 kHz. In this case, the DC gain from V_{in} to I_{in} without the compensator $E(z)$ becomes 0.122.

B. Root map

Figure 8 shows the location of the poles and zeros. Zeros shown in Figure 8 are those from V_{in} to I_{in}. Crosses and circles

Table 1 Circuit parameters

	Symbol	Value
Filter inductance	L_f	2.07 mH
Filter capacitance	C_f	18.4 μF
Inductance of the inner inductor	L	591 μH
Control period	T	100 μs
Switching frequency	f_{sw}	10 kHz
DC bus voltage	V_{bus}	100 V
Dead time	τ_d	500 ns

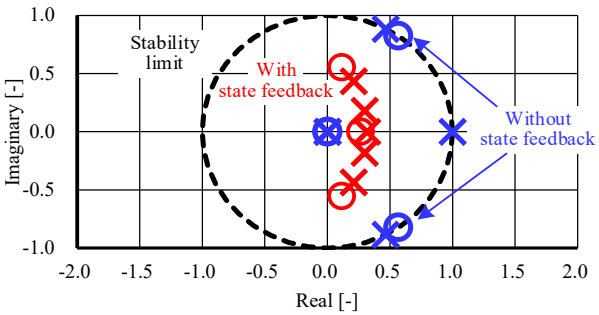
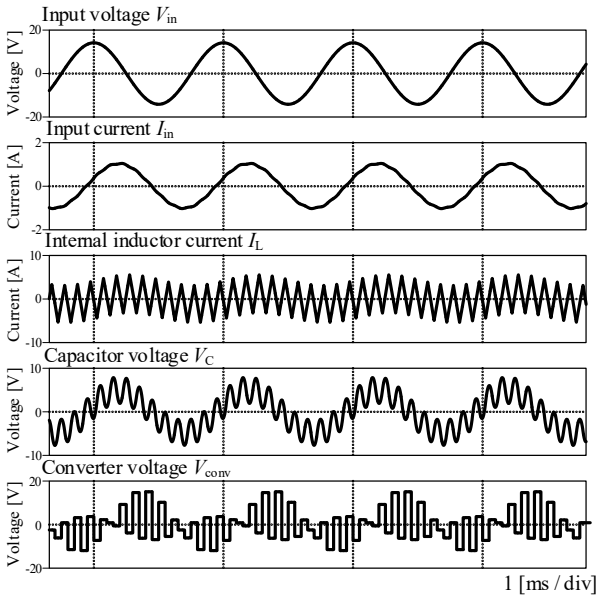


Fig. 8. Root map after/before state feedback

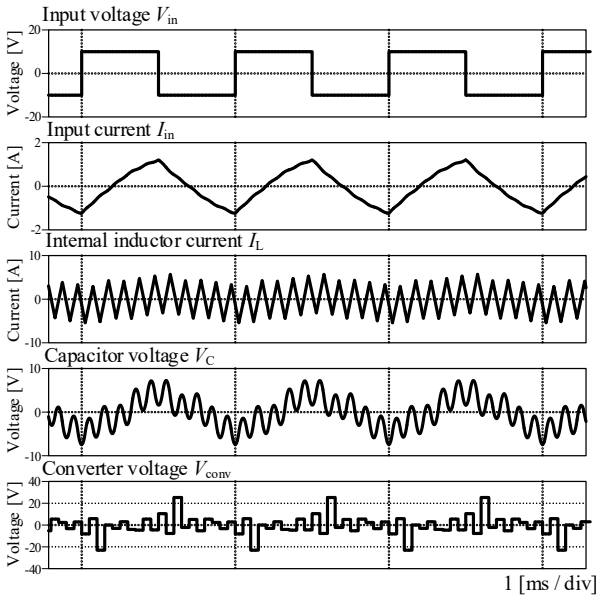
indicate poles and zeros, respectively. Blue points show the roots of the natural LCL plant. Red points show the roots of the modified plant. The natural plant shown in blue points has three poles on the stability limit. Among these poles, the pole on the real axis indicates the integrator mode. On the other hand, other poles on the stability limit indicate the resonance mode. By applying state feedback, all poles and zeros are specified inside the stability limit.

C. Transient response

Figure 9 shows the operation waveform of the virtual impedance circuit in the simulation. The switching frequency of the virtual impedance circuit is set to 10 kHz. The target emulation inductance is set to 3.9 mH. In Figure 9(a), a sinusoidal input voltage is applied. The amplitude of V_{in} is set to 10 V_{rms}. The waveforms indicate, from the top, the input voltage V_{in}, the input current I_{in}, the internal inductor current I_L, the capacitor voltage V_C, and the converter output voltage V_{conv}. In this condition, the V_{in} frequency is set to 1 kHz. The



(a) Sinusoidal input voltage



(b) Square wave input voltage

Fig. 9. Virtual impedance operation in the simulation.

phase difference between V_{in} and I_{in} is around 90 degrees. Therefore, the fundamental virtual impedance operation is confirmed. In Figure 9(b), a square wave input voltage is applied. The input frequency is also set to 1 kHz. In this case, the input current Iin should be a triangular wave; however, a slight distortion is observed. This distortion is mainly attributed to the phase error of the proposed control.

D. Variable inductance operation

Figure 10 shows the variable inductance operation waveform. Input current is reduced seamlessly against the same input voltage during the operation. The emulation inductance is changed from 1.30 mH to 3.76 mH.

E. Frequency characteristics

Figure 11 shows the frequency characteristics of the transfer function from V_{in} to I_{in} for the conventional and proposed controls in the simulation. This plot is obtained by using numerical analysis. The blue and red lines indicate the conventional and proposed controls, respectively. The frequency of input voltage V_{in} is normalized by the switching frequency. In the case of conventional control, the gain characteristic is flat; however, the phase characteristic worsens in the high-frequency region. This is because conventional control has a constant group delay. When the input frequency reaches 0.13 times the switching frequency, the phase exceeds 180 degrees in the conventional control. This means that the emulated impedance exhibits the opposite

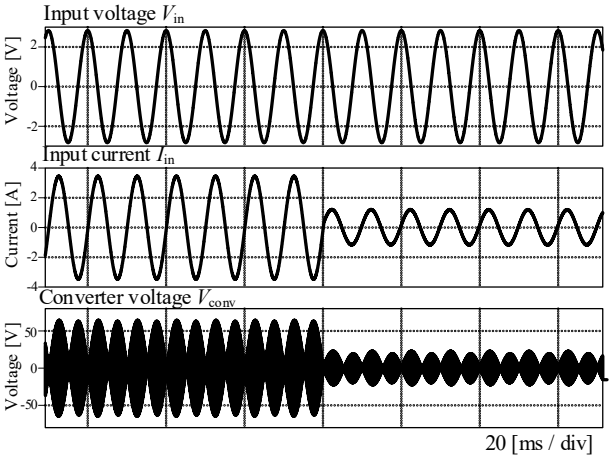


Fig. 10. Variable inductance operation waveform.

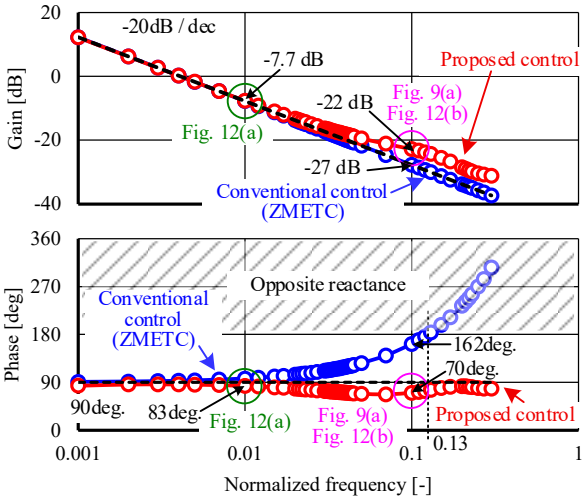


Fig. 11. Comparison of frequency characteristics of conventional / proposed controls in the numerical analysis.

reactance characteristic. On the other hand, in the phase characteristic, the proposed control maintains around 90 degrees even as the input frequency approaches the switching frequency. Therefore, the proposed control is shown to improve the phase characteristic and extend the operable frequency range.

V. Experimental Results

Figure 12 shows the operating waveform of the virtual impedance circuit. The target emulation inductance $L_{emu.}$ is set to 3.9 mH. In Figure 12(a), the input voltage V_{in} is set to 3 V_{rms}. The input frequency is 100 Hz. The amplitude of the input current I_{in} is 2.0 A. In this condition, the active and reactive current components are 0.618 A and 1.90 A, respectively. The calculated emulation inductance is 3.55 mH. Moreover, a slight distortion is observed in I_{in}. This is because the input voltage is low relative to the full-scale range of the detection circuit, and even a slight detection error becomes significant under this condition. In Figure 12(b), the input voltage V_{in} is set to 10 V_{rms}. The input frequency is 1 kHz. The voltage amplitude and frequency are set to the same values as those used in Fig. 9(a). The amplitude of the input current is 1.4 A. In this condition, the active and reactive current components are 0.433 A and 1.33 A, respectively. The calculated emulation inductance is 1.69 mH. The magnitude and phase of the input current agree well with the simulation results shown in Figure 9(a). Although the phase relationship still indicates inductive behavior, the emulated inductance deviates significantly from the target value. This deterioration in emulation accuracy is presumably related to the cutoff-frequency setting of the Bessel low-pass filter and its sensitivity to parameter mismatches. In general, a higher cutoff frequency makes the system more sensitive to parameter variations. There is a trade-off relationship between system robustness and performance.

Therefore, the experimental results indicate that virtual inductive behavior can be maintained up to an input frequency corresponding to 10% of the switching frequency, although the emulation accuracy deteriorates in the high-frequency region. The experimental results are consistent with the improved phase characteristics predicted for the proposed control.

VI. Conclusion and Future Work

This paper proposed a control method for broadband virtual impedance circuits. Simulation and experimental results indicate that the proposed control extends the frequency range over which virtual inductive behavior is maintained, compared with the conventional method. Experimental verification was carried out at an input frequency corresponding to 10% of the switching frequency. Although inductive behavior was maintained under this condition, a noticeable emulation error remained in the high-frequency region. These results suggest that the proposed method improves the phase characteristics of the virtual impedance circuit, while further improvements in modeling accuracy and implementation are required.

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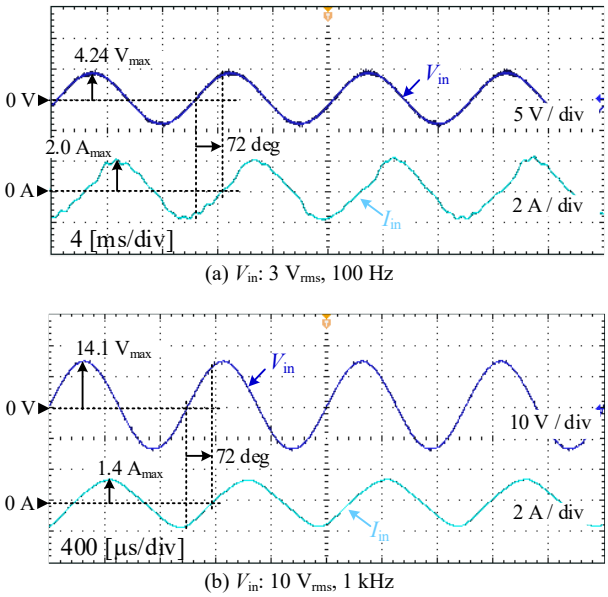

(a) V_{in}: 3 V_{rms}, 100 Hz

(b) V_{in}: 10 V_{rms}, 1 kHz

Fig. 12. Operating waveform of the virtual impedance circuit.

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