

Transformer-Current Minimization in a Center-tap DAB Matrix Converter with Turns-Ratio Design

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Abstract— This paper proposes a center-tapped dual-active-bridge matrix converter with integrated active power decoupling for single-phase/three-phase compatible chargers. In the proposed circuit, the transformer secondary center-tap is used to absorb single-phase power pulsations without additional switching devices. The differential period is analytically formulated as a function of the grid phase, and the feasible operating range satisfying both pulsation compensation and power transfer is derived. Based on this range, design guidelines for the buffer capacitance and transformer turns ratio are established, and a turns-ratio condition for minimizing transformer current is clarified. Experimental results show that the proposed method reduces the second-order DC-current ripple component by 89.5% without increasing the transformer RMS current.

Keywords— Matrix Converter, Dual Active Bridge, Center-tap, Active power decoupling

I. INTRODUCTION

Recently, charging infrastructure has become increasingly diverse as EV adoption has grown. Public fast chargers primarily use a three-phase grid, whereas residential applications typically use single-phase. Therefore, on-board chargers (OBCs) must support both power sources. Furthermore, it is important to achieve both galvanic isolation from the grid and bidirectional power transfer as vehicle-to-grid (V2G) technology advances [1].

In three-phase/single-phase dual-compatible circuits, power pulsation compensation is necessary during single-phase operation. To compensate for the pulsation, active power decoupling (APD), which actively controls the buffer current using semiconductor switches, improves reliability by eliminating electrolytic capacitors and has been integrated into many three-/single-phase dual-purpose OBCs [2-4]. However, two-stage topologies, which consist of a power factor correction AC-DC converter and an isolated DC-DC converter, require additional passive components, such as boost inductors and DC-link capacitors, whereas modular topologies still face issues with component count and redundancy.

On the other hand, the matrix converter, which does not require an energy storage stage, has attracted attention as a topology that can realize a configuration without bulky passive components. Conventional studies have proposed a method that places a half-bridge on the DC side and reuses the inductor of the EV motor as an energy-storage element to compensate for power pulsation [5]. However, an inductor reduces efficiency due to copper losses and requires additional switches for the APD. To address this issue, another approach has been studied in which a buck-type APD is formed by using the leg that remains inactive under single-phase connection, and pulsation compensation is achieved without additional switches [6]. However, when the current variation range of the

buffer capacitor is increased, the conduction loss due to the on-resistance increases because the bidirectional switches operate as a half-bridge. As a result, a capacitance comparable to that required for passive pulsation compensation is still needed, which limits system size reduction. Another method has been proposed that reuses the grid-disconnected leg and the LC elements of the input filter in the APD circuit[7]. Although this approach enables compensation without additional components, strict constraints are imposed on the DC voltage and switching frequency to compensate for pulsation while canceling the leading current of the capacitor connected in parallel with the grid.

This paper proposes a center-tapped dual-active-bridge matrix converter with integrated active power decoupling to enable converter miniaturization. In the proposed circuit, a buffer capacitor and a smoothing inductor are connected to the center-tap of the DC-side transformer winding. The buffer capacitor is charged and discharged simultaneously with power transmission, which is controlled during the common-mode and differential-mode periods. In this way, APD is achieved without adding extra switching devices.

The originality of this paper lies in proposing and analyzing a center-tapped DAB matrix converter with integrated active power decoupling. In particular, the configuration-specific trade-off between APD capability and power-transfer capability is analytically clarified. The buffer capacitor voltage is controlled by adjusting the common-mode period imbalance in the proposed circuit. However, increasing the imbalance ratio to enlarge the buffer current introduces distortion in the grid current. This imposes a design trade-off between the imbalance ratio, limited by the grid current THD constraint, and the capacitance, which must be increased accordingly. Furthermore, introducing imbalance into the common-mode period may increase the transformer current [8-9].

To address these issue, this paper analytically derives the feasible operating range of the differential period that satisfies both the single-phase power pulsation compensation and power transfer requirements. In addition, the differential period that minimizes the RMS transformer current is identified within the feasible range. Based on the analysis, quantitative design guidelines for the buffer capacitance and transformer turns ratio are established. The effectiveness of the proposed method is verified through simulation and experiments.

II. CIRCUIT CONFIGURATION

Fig. 1 shows the proposed circuit. The circuit employs a center-tapped transformer, and the primary side is connected to the grid via a matrix converter. Bulky passive components are not required when using a matrix converter. The

secondary-side inverter controls power in the differential period and charges and discharges the buffer in the common-mode period during single-phase operation. In particular, the common-mode period consists of charging and discharging patterns with upper- and lower-arm states. The average center-tap voltage can be controlled by the imbalance in these patterns. This inverter control eliminates the need for an additional switch. Moreover, implementing the buffer on the DC side enables efficient ripple suppression by leveraging the high DC voltage without affecting the power factor. In three-phase grid-connected operation, a high power factor is achieved through grid current control based on space-vector modulation [10].

III. ACTIVE POWER DECOUPLING WITH CENTER-TAP

The proposed control aims to transmit power while generating the necessary center-tap voltage for pulsation absorption. Since unbalanced charge/discharge ratios limit transferable power and increase voltage ripple, the buffer capacitor C_{buf} must be sized to manage this imbalance. Additionally, the transformer turns ratio N affects the voltage-time product, directly altering the transferable power even when the differential period remains constant. Therefore, this study defines the feasible operating range of the differential period by considering both C_{buf} and N . Following a description of the switching-based voltage generation, the transmitted power is formulated to establish design guidelines for C_{buf} and N , aiming to minimize transformer current and converter size.

A. Switching Patterns of the DC-Side Inverter

Fig. 2 shows the transformer voltage waveforms for each switching pattern and the center-tap voltage v_{com} . The primary side transformer voltage v_{mc} is always a square wave. The secondary side voltage v_{inv} is a three-level waveform that includes a common-mode period, introduced by the differential output period φ between the legs. The conduction period of the upper arm is defined as α . When α is not equal to 0.5, v_{inv} becomes asymmetric within a switching period. The parameter δ is defined as the phase difference between primary and secondary carriers. This δ differs from the fundamental phase shift used in conventional single-phase shift control because of the asymmetry of v_{inv} .

The secondary-side output voltage alternates between charging and discharging modes while maintaining differential voltage patterns. This arrangement enables both buffer current control and power transfer within a single switching period. Furthermore, to suppress biased magnetization and to ensure that the secondary-side inverter outputs a differential voltage, the constraints on α and φ are given by

$$\varphi \leq 2\pi\alpha \leq 2\pi - \varphi \quad (1).$$

B. Power Pulsation Compensation by Common-Mode

In a single-phase grid with a unity power factor, the instantaneous power p_g is expressed by

$$p_g = V_g I_g \{1 - \cos(2\omega_g t)\} = P_{avg} - P_{avg} \cos(2\omega_g t) \quad (2).$$

Here, I_g is the rms grid current, P_{avg} is the power, and ω_g is the grid angular velocity.

The second term in (2) denotes the power pulsation to be compensated. To absorb this energy deviation, the

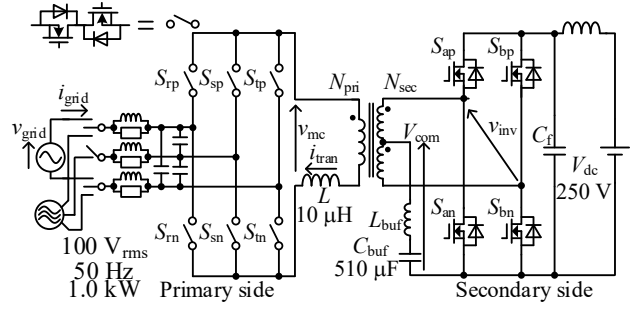


Fig. 1. DAB-type matrix converter with center-tap.

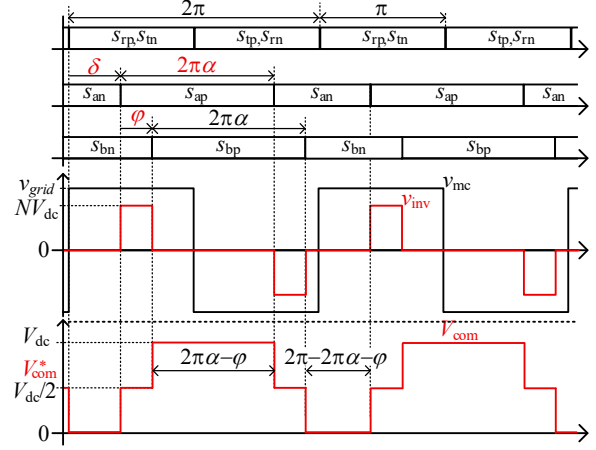


Fig. 2. Relationship between the transformer voltage waveform, the switching patterns and the center-tap voltage waveform.

instantaneous buffer capacitor voltage v_{Cbuf} is derived from the energy balance equation as

$$v_{Cbuf} = \sqrt{\left(\frac{V_{dc}}{2}\right)^2 + \left(\frac{P_{avg}}{V_{dc}\omega_g C_{buf}}\right)^2} - \frac{P_{avg}}{\omega_g C_{buf}} \sin(2\omega_g t) \quad (3).$$

Within the range defined by (1), the center-tap voltage v_{com} is the average voltage applied to the center-tap over one switching period and is given by

$$V_{com} = \frac{1}{2\pi} \left\{ (2\pi\alpha - \varphi)V_{dc} + 2\varphi \frac{V_{dc}}{2} + (2\pi - \alpha - \varphi) \cdot 0 \right\} = \alpha V_{dc} \quad (4).$$

C. Proposed Control Block Diagram

Fig. 3 shows the proposed control block diagram. In the proposed control, the conduction period α is determined by the average control of the buffer capacitor and the ripple-current control for APD. In addition, the differential period φ is preset for each grid phase to minimize the RMS transformer current while taking the transformer turns ratio N into account. The phase shift δ and current mode are determined from α and φ to satisfy the power command.

IV. TRANSMITTED POWER CONSIDERING THE CENTER-TAP

A. Pulse pattern of Transformer voltage

Fig. 4 lists the current modes and their operating conditions. While 16 modes exist as δ varies from 0 to 2π , several are unsuitable for practical use. Specifically, $\delta > \pi$ induces excessive circulating current due to high voltage across the leakage inductance. Furthermore, some modes exhibit power transfer independent of δ , making them

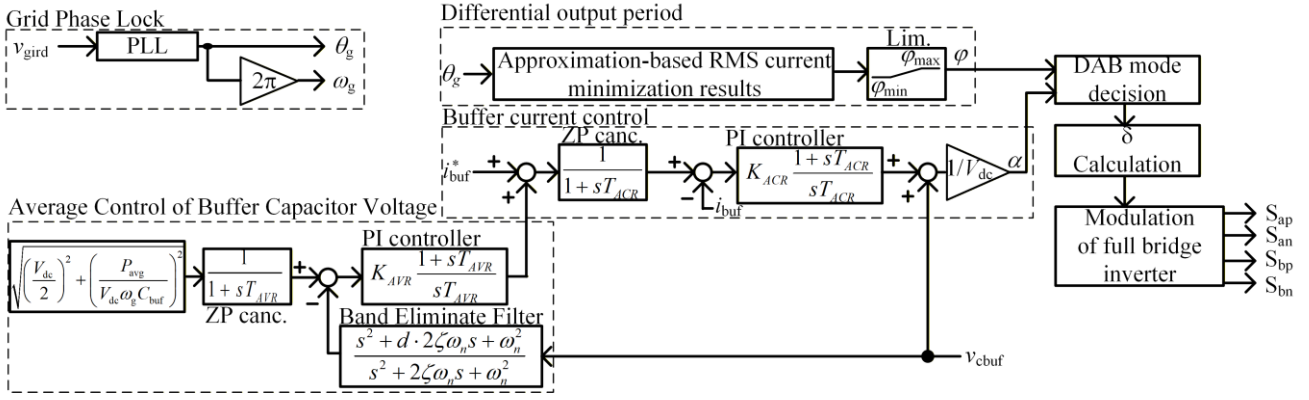


Fig. 3. Block diagram of the proposed buffer current control and transformer current minimization control.

ineffective for control. Consequently, these modes are excluded, leaving six modes for operation.

B. Relationship between Control Parameters and Power

The active power of the DAB is obtained by averaging the product of the transformer current and the transformer voltage over one switching period. For the current mode E shown in Fig. 4(e), the relationship between the transmitted power and the three control parameters is expressed by

$$p_g = \frac{NV_{dc}|v_{grid}|}{\pi\omega_{sw}L} \left(\frac{1}{4}\pi^2 - \left(\delta + \frac{\phi + 2\pi\alpha - 3\pi}{2} \right)^2 - \pi^2 \left(\alpha - \frac{1}{2} \right)^2 - \frac{1}{4}(\phi - \pi)^2 \right) \quad (5).$$

Thus, the phase difference δ that achieves the desired power command is obtained by solving (5), as shown in

$$\delta = 2\pi(1 - \alpha) - \frac{\sqrt{2\pi}}{NV_{dc}|v_{grid}|} \sqrt{\left(\phi - \alpha\phi \right) - \frac{2\pi L f_{sw}}{NV_{dc}|v_{grid}|} p_g^*} \quad (6).$$

The relationship between the control parameters and the transmitted power is derived using the same procedure for the other modes. Based on the derived values of δ , α , and ϕ , the mode that satisfies the mode determination conditions is selected.

V. DIFFERENTIAL PERIOD FOR MINIMIZING TRANSFORMER CURRENT

A. Clarification of the Feasible Operating Region of the Differential Output Period

Fig. 5 shows the differential period ϕ and the current mode region. In the proposed method, ϕ is subject to two constraints. First, the upper limit of ϕ is restricted by the APD operation. Based on (1) and (4), the buffer capacitor voltage determines the upper-arm conduction period α , and the maximum value of ϕ is defined within the range that does not interfere with α . Therefore, the upper limit ϕ_{max} is given by

$$\phi_{max}(t) = 2\pi \min(\alpha(t), 1 - \alpha(t)) \quad (7).$$

APD is prioritized over power transmission in this control method. Therefore, ϕ is limited to ϕ_{max} when the differential output period ϕ tends to exceed ϕ_{max} .

Next, the lower limit of ϕ is determined by the transmitted power. In single-phase operation, the power fluctuates instantaneously. Therefore, ϕ must satisfy the power command at each grid phase. The power transfer characteristic depends on the current mode. However, it is difficult to

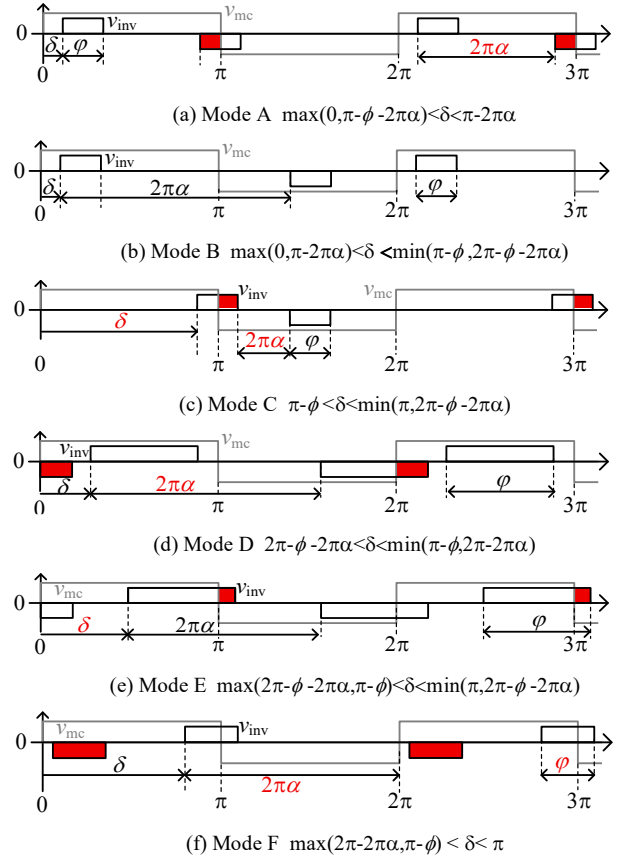


Fig. 4. Transformer voltage and current waveforms and the corresponding control-parameter magnitude relationships.

analytically identify the mode that gives the minimum ϕ over the entire grid phase. Therefore, the proposed control defines the lower limit of ϕ as ϕ_{min} based on the current mode E. In this case, ϕ_{min} is given by

$$\phi_{min}(t) = \pi - 2\sqrt{\pi} \sqrt{\pi\alpha(1 - \alpha) - \frac{\omega_{sw}L}{NV_{dc}|v_{grid}|} p_g} \quad (8).$$

If the differential output period ϕ satisfies $\phi_{min} \leq \phi < \phi_{max}$, the desired power transfer and APD operation are achieved simultaneously since the converter can operate in one of the current modes shown in Fig. 4.

B. Quantitative Design Guidelines for the Buffer Capacitance and Transformer Turns Ratio

Given the input and output voltages, the buffer capacitance C_{buf} determines the buffer capacitor's voltage fluctuation due to power pulsation. The differential period ϕ must be adjusted to match the voltage fluctuation. The transformer turns ratio N determines the amplitude of the differential output voltage. It changes the time integral of the differential output voltage without changing ϕ . Therefore, C_{buf} and N are the main design parameters that define the allowable range of ϕ . The selection of these parameters is important for establishing APD, meeting the required power transfer, and reducing the RMS value of the transformer current. This section presents design guidelines for C_{buf} and N based on the relationship between the allowable ϕ range and the transformer RMS current.

To satisfy the condition $\phi_{\min} \leq \phi < \phi_{\max}$ over the entire grid phase based on the APD upper limit in (7) and the required $\phi_{\min}$ in (8), the transformer turns ratio N is derived as

$$N = \max \left(\frac{2\sqrt{2}\omega_{\text{sw}}L_{\text{avg}}P_{\text{avg}}/V_{\text{dc}}}{\pi V_{\text{dc}}}, \frac{|\sin(\omega_{\text{g}}t)|}{1/2 - 4\alpha(t)(1-\alpha(t))} \right) \quad (9).$$

Using (9), the required N for a given C_{buf} can be determined quantitatively. This enables a theoretical basis for miniaturized design based on the theoretical limits.

Fig. 6 shows the feasible operating boundary for C_{buf} and N under the desired power conditions. The analysis conditions are the same as the experimental conditions listed in Table 1, and the buffer capacitor voltage is assumed to vary from 20% to 80% of the DC voltage. The vertical axis is normalized to the capacitance required for the buck-type APD circuit to satisfy the same voltage variation condition. Fig. 6 shows that the center-tap APD circuit can achieve power pulsation compensation with a capacitance comparable to that of the buck-type APD circuit while eliminating additional APD switches. by appropriately selecting N . In addition, the region above the boundary represents the design range in which both power pulsation compensation and power transfer can be satisfied simultaneously.

C. Minimization of the Transformer Current RMS Value

The differential period ϕ is adjusted to satisfy the power command while minimizing the instantaneous current relative to the grid voltage to minimize the RMS transformer current. Fig. 7 shows the RMS current distribution and its minimum trajectory. In the high-voltage region, ϕ is limited by APD requirements, as constrained by (7). Conversely, in the low-voltage region where this margin is sufficient, the trajectory follows a minimum path derived from numerical analysis.

Fig. 8 shows the variation of the transformer RMS current obtained by simulation when C_{buf} is fixed at 510 μF and the turns ratio N is varied. The simulation conditions are the same as those in Table 1. The RMS reaches a minimum of 13.3 A_{rms} at the turns ratio of 0.565, where the peak grid voltage equals the primary-referred DC voltage, NV_{dc} . In the region where the peak grid voltage exceeds NV_{dc} , the differential period ϕ reaches the maximum value $\phi_{\max}$ given by (7), and ϕ can no longer be adjusted according to the grid voltage. As a result, the rms current increases.

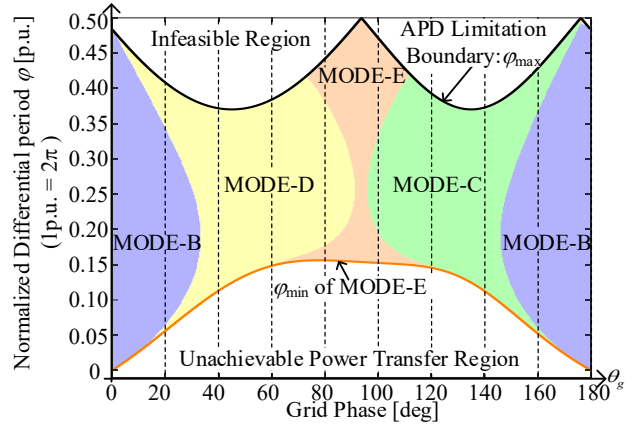


Fig. 5. Feasible operating region of the differential output period considering APD and transmitted power.

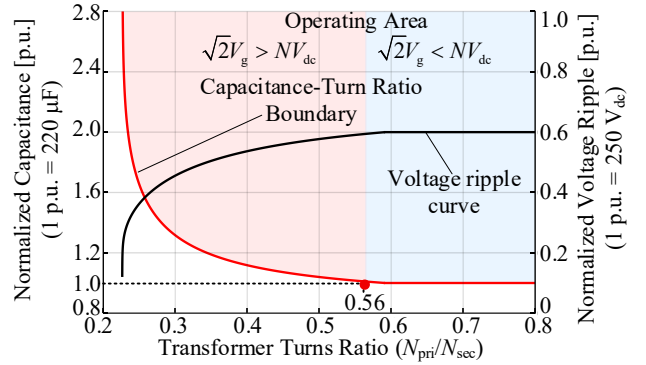


Fig. 6. Relationship between turns ratio and buffer capacitance.

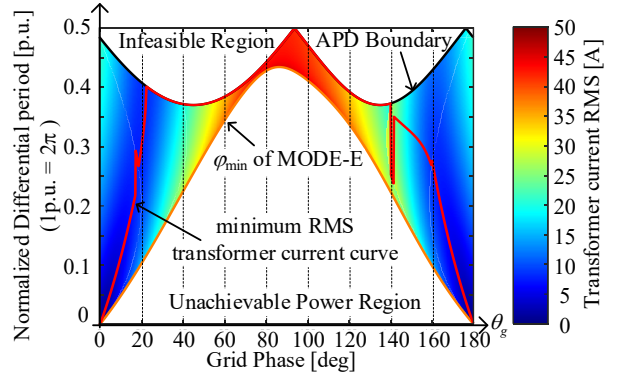


Fig. 7. Variations of the transformer RMS current and the minimum transformer current as a function of the grid phase.

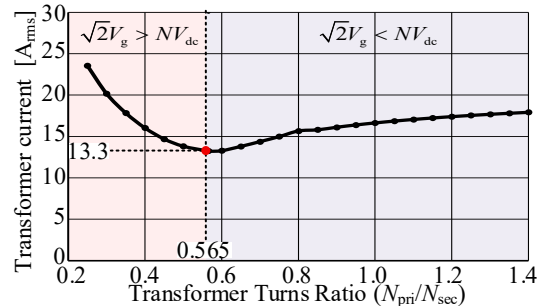


Fig. 8. Variation of transformer RMS current with turns ratio at a fixed buffer capacitance.

VI. EXPERIMENTAL VERIFICATION

Table 1 summarizes the experimental conditions. A single-phase 100 V_{rms} grid connection is assumed. The buffer

Table 1. Circuit parameters

Conditions	Symbol	Value
Switching frequency	f_{sw}	50 kHz
Power	P_{avg}	1.0 kW
Grid voltage	v_{grid}	100 V _{RMS}
Grid frequency	f_g	50 Hz
AC filter capacitor	$C_{ac}(\%Y)$	6.6 μ F (2.1%)
Buffer capacitor	$C_{buf}(\tau_c)$	510 μ F (32 ms)
DC-source voltage	V_{dc}	250 V
DC filter capacitor	$C_f(\tau_c)$	25 μ F (1.6 ms)
Leakage inductor	L	10 μ H
Turn ratio(Pri.:Sec.)	N	0.6:(1:1)

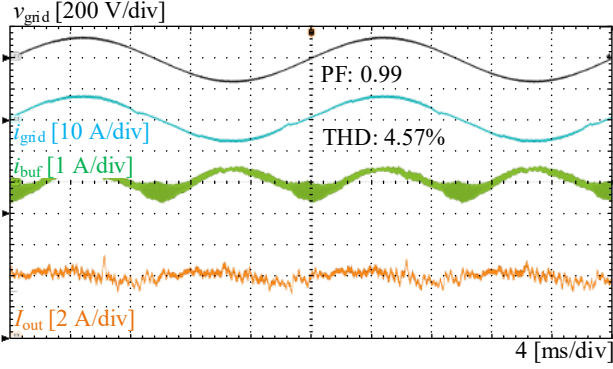


Fig. 9. Experimental waveforms under the conditions listed in Table 1.

capacitance is 510 μ F, and the turns ratio is set to 0.3, which is above the boundary line shown in Fig. 6.

Fig. 9 shows the input and output waveforms and the current waveforms of the buffer capacitor when power pulsation compensation is applied. The results indicate that the buffer capacitor current i_{buf} fluctuates to absorb the power pulsation, thereby keeping I_{dc} almost constant. The total harmonic distortion (THD) of the grid current is 4.57%, and the grid power factor is 0.99.

Fig. 10 shows the frequency analysis results for the DC current with and without the proposed pulsation compensation. In harmonic analysis, the 50 Hz output frequency is defined as the fundamental component. Compared with the case without power pulsation compensation, the proposed method reduces the second-order harmonic component by 89.5%.

Fig. 11 compares the transformer voltage and current waveforms. The transformer current was 18.6 A_{rms}, which is 2.9% lower than without the proposed method under the same operating condition. Furthermore, the result agrees well with the analytical value, with an error of 9.2%, which confirms that the proposed method functions properly.

The input and output voltage conditions were changed to verify the operating point that minimizes the transformer RMS current. In this verification, the grid voltage was set to 100 V_{ac} and the DC voltage was set to 471 V_{dc} so that the peak grid voltage matched the primary-referred DC voltage.

Fig. 12 shows the operating waveforms under the condition that minimizes the transformer RMS current. Fig. 12(a) shows the waveforms for the case in which only the average voltage control of the buffer capacitor is applied. In this case, the buffer capacitor voltage remains nearly constant.

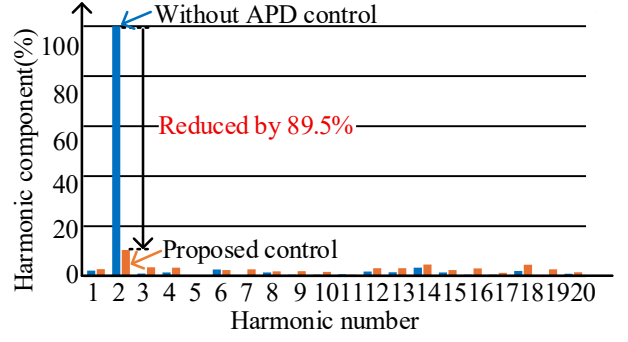
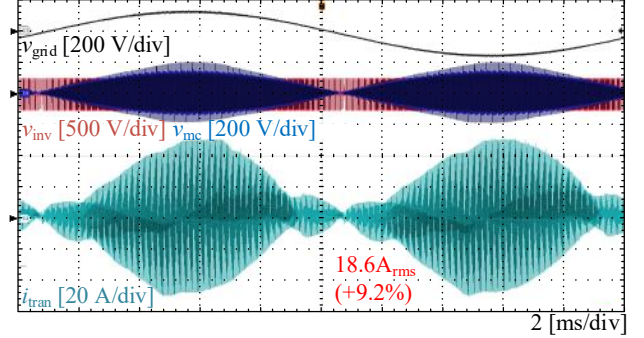


Fig. 10. Frequency analysis results of the DC current with and without power pulsation compensation under the conditions listed in Table 1.

Fig. 11. Transformer voltage and current waveforms obtained with the transformer RMS current minimization method at a grid voltage of 100 Vac and DC voltage of 250 V_{dc}, and comparison with the analytical transformer RMS current.

Therefore, the second-order frequency component is superimposed on the DC-side current. On the other hand, as shown in Fig. 12(b), the proposed power pulsation compensation method causes the buffer capacitor voltage to fluctuate and reduces the ripple in the DC current. In this case, the differential period follows the transformer-current minimization method derived as shown in Fig. 7. Consequently, the switching ripple amplitude of the buffer current changes with a period of 100 Hz.

The ripple reduction is limited to 76.4%, mainly because the dead time in the DAB causes a power transfer error. As shown in Fig. 12, distortion is observed in the grid current waveform near the peak of the grid voltage. Consequently, the total harmonic distortion (THD) increases, and a power imbalance occurs between the buffer power and the actual power fluctuation.

Fig. 13 shows a comparison of the transformer RMS current with and without power pulsation compensation. In Fig. 13(a), only the average voltage control of the buffer capacitor is applied. Therefore, the common-mode periods remain balanced. On the other hand, in Fig. 13(b), the common-mode period is varied according to the grid phase to achieve power pulsation compensation. The transformer RMS current obtained using the same analytical method as in Fig. 8 was 11.55 A_{rms}, whereas the measured value in Fig. 13(b) was 11.90 A_{rms}. The error with respect to the analytical value was 3.0%. The experimental result agrees well with the analytical result even at the operating point where the transformer current is minimized. These results confirm the validity of the proposed method. In addition, the transformer RMS current in Fig. 13(a) was 12.24 A_{rms}, which is comparable to the value of 11.90 A_{rms} in Fig. 13(b). Therefore, it is confirmed that the

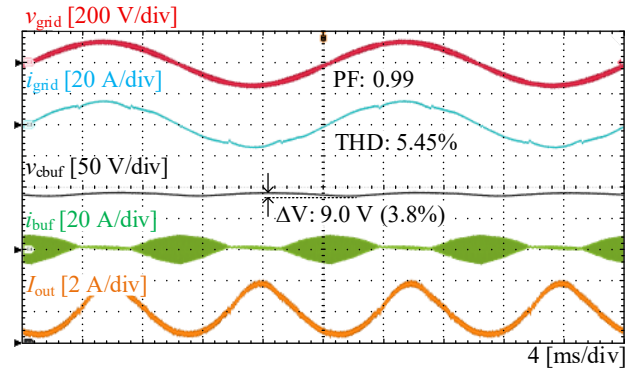
proposed power pulsation compensation method does not increase the transformer RMS current.

VII. CONCLUSION

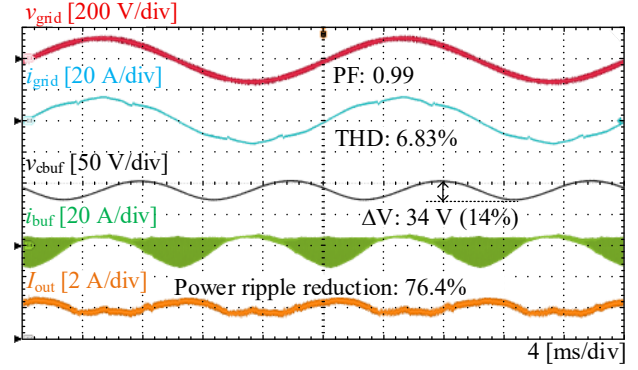
This paper proposed a transformer-current minimization method for a center-tapped DAB matrix converter with integrated active power decoupling. The feasible operating region of the differential output period was analytically derived to satisfy both power pulsation compensation and power transfer. Based on this region, design guidelines for the buffer capacitance and transformer turns ratio were presented, and the differential period that minimizes the RMS transformer current was determined. The analysis showed that the transformer RMS current is minimized when the turns ratio is selected such that the peak grid voltage equals the primary-referred DC voltage. Experimental results demonstrated that the proposed method reduced the second-order DC-current ripple component by 89.5% while maintaining a grid-current THD of 4.57%. In addition, the transformer RMS current with power pulsation compensation was comparable to that without compensation, confirming that the proposed method achieves power pulsation compensation without increasing the transformer RMS current or requiring additional switches.

REFERENCES

- [1] A. Ali, H. H. H. Mousa et al. "A Comprehensive Review on Charging Topologies and Power Electronic Converter Solutions for Electric Vehicles" *Journal of Modern Power Systems and Clean Energy*, vol. 12, no. 3, pp. 675-694, 2024
- [2] B. P. Do, M. Gerado Geda, H. -P. Kieu and S. Choi, "A Half-Bridge Single-Stage AC-DC Converter With Single- and Three-Phase Compatibility," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 13, no. 6, pp. 8051-8061, Dec. 2025
- [3] J. Lee, T. -T. LE, H. Kim and S. Choi, "A Compact 17.6 kW Single-/22 kW Three-Phase Compatible EV Charger: Analysis of Active Power Decoupling, Wide Voltage Range Operation," in *IEEE Transactions on Industrial Electronics*, vol. 72, no. 8, Aug. 2025
- [4] H. Kim, J. Park, S. Kim, R. M. Hakim, H. Belkamel and S. Choi, "A Single-Stage Electrolytic Capacitor-Less EV Charger With Single- and Three-Phase Compatibility," in *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6780-6791, June 2022
- [5] A. R. P. A. Sridhar and N. Weise, "DC ripple current rejection in a bidirectional SiC single-phase AC-DC converter for V2G application," 2015 IEEE Transportation Electrification Conference and Expo (ITEC), Dearborn, MI, USA, 2015
- [6] S. Barman, S. Chakraborty and K. Chatterjee, "High Frequency Link Ripple Power Compensation Strategies for 1- ϕ Bidirectional AC-DC Matrix Converters," *ECCE Asia*, Jeju Island, Korea, Republic of, 2023
- [7] M. Ishii, S. Komeda, S. Takuma and Y. Ohnuma, "A Power Decoupling Control Method for a Matrix Converter-Based DAB AC-DC Converter," 2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE), Philadelphia, PA, USA, 2025
- [8] J. You, D. M. Vilathgamuwa, N. Ghasemi and W. L. Malan, "An Active Power Decoupling Method for Single Phase DC/AC DAB Converters," in *IEEE Access*, vol. 7, pp. 12964-12972, 2019
- [9] P. Yang et al., "Optimal Dual-Side Asymmetric Modulation Strategy for Dual Active Bridge Converter to Improve Efficiency Over a Wide Voltage Range," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 2, pp. 1596-1607, April 2024
- [10] S. Takuma, K. Kiri, H. Watanabe and J. Itoh, "Surge Voltage Reduction Method for DAB Matrix Converter using Circulating Current in Whole Load Condition," *ECCE*, 2301-2307, 2021

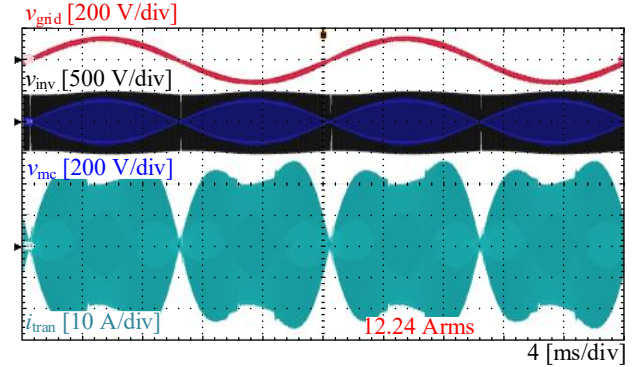


(a) With only average buffer-capacitor voltage control.

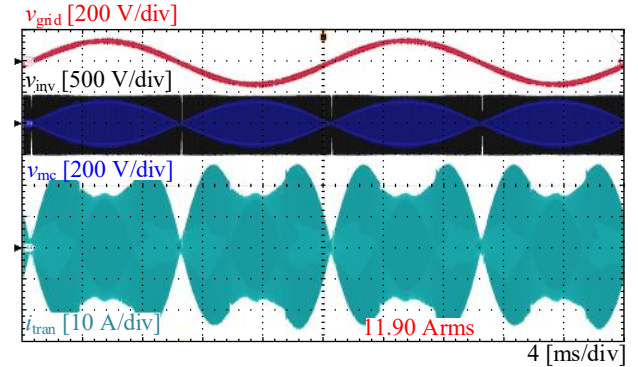


(b) With the proposed power pulsation compensation method.

Fig. 12. Input and output waveforms at the operating point that minimizes the transformer RMS current under a grid voltage of 100 V_{ac} and a DC voltage of 471 V_{dc}.



(a) Without power pulsation compensation.



(b) With power pulsation compensation.

Fig. 13. Transformer voltage and current waveforms at the operating point that minimizes the transformer RMS current under a grid voltage of 100 V_{ac} and a DC voltage of 471 V_{dc}.